

lecture 7: system clock

1.introduction

2.memory control signal

3. minimum mode

4. maximum mode

1. INTRODUCTION

The 8086 microprocess is manufactured in three speeds: the 5-MHz 8086, the 8-MHz 8086-2 and 10-MHz 8086-1. The 8284 clock generator and driver IC generate CLK, shown in figure (1).

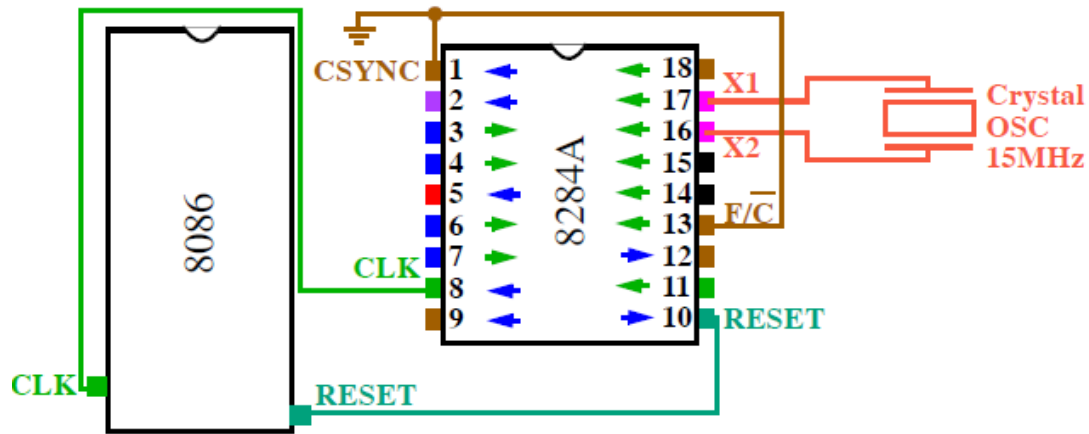


Figure 1: block diagram 8284 clock generator

The 8284 outputs the crystal frequency as oscillator (OSC) frequency, one third of crystal frequency as clock (CLK) frequency and half of clock frequency as peripheral (PCLK) clock frequency. Thus, if a 8284 clock generator IC is supported by a 15 MHz crystal oscillator frequencies, such as, Oscillator frequency of 15 MHz, clock frequency of 5 MHz and peripheral clock frequency of 2.5 MHz . A bus-cycle defines the basic operation process of a microprocessor to communicate with external devices. Such as, memory read bus-cycle, where data stored in main memory is read into the internal registers of the CPU (such as AX).- Typically, the bus-cycle of the 8086 and 8088 processors consist of four clock cycles or pulses. Thus, duration of a bus-cycle is = $4 \cdot T$. A bus-cycle involving a data transfer operation between the CPU and external storage device (memory) is shown in the figure (2).

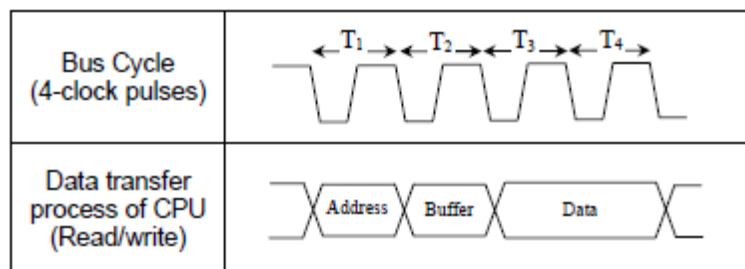


Figure 2: bus cycle

during time state ‘T1’, the microprocessor puts the address on the system-bus and writes or reads data during time states ‘T3’ and ‘T4’ and During the absence of bus activity or bus-cycles, the processor performs what are known as “ideal-states”. Each ideal-state is one CLK period long and any number of them can be inserted between bus-cycles, as shown in figure (3).

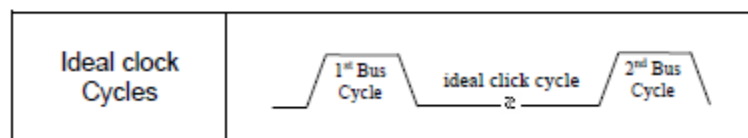


Figure 3: ideal clock cycle

ideal-states are performed when the instruction queue inside the microprocessor becomes full and their execution does not involve any memory or input/output operands. Often the microprocessor requires interfacing with slower memory and input/output devices and needs to prolong its bus-cycle by inserting “wait-states” between the time states ‘T3’ and ‘T4’, as long as the slower external device keep supplying logic “0” to the “Ready” pin of 8088/8086 CPU. wait –state as show in figure (4).

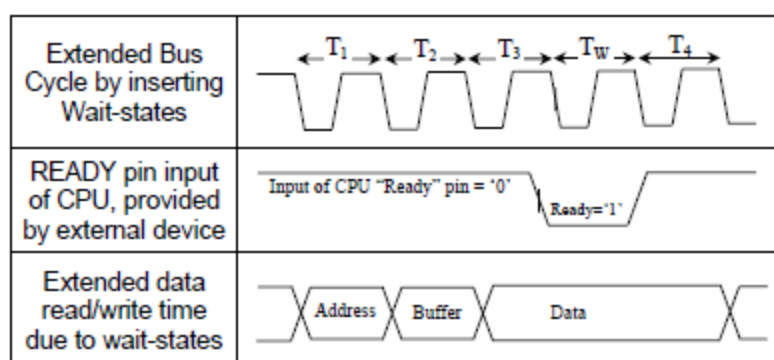


Figure 4: wait-state addition.

2. MEMORY CONTROL SIGNAL

in the minimum mode, the 8088 and 8086 microprocessor on produce all the control signals. But in the maximum mode, the 8288 bus controller produces them. In the 8086 microcomputer system which is configured for the minimum mode to support the interface to the memory subsystem are ALE, IO/M, DT/R, RD,WR. And DEN.

- Address latch enable (ALE) signals external circuit y that a valid address is on the bus. It is a pulse to the I logic level and is used to latch the address in external circuitry.
- The input-output/memory (IO/M) external circuitry whether a memory or I/O bus cycle is in progress , During all memory bus cycles (read/write), IO/M is held at the 0 logic level .
- data transmit/receive (DT/R) is Logic 1 during the data transfer part of the bus cycle, the bus is in the transmit mode, and data are written into memory On the other hand, it sets DT/R to logic 0 to signal that the bus is in the receive mode, which corresponds to reading of memory.
- Read (RD) identify read bus cycle ,RD logic to 0 to signal memory
- write (WR) identify write bus cycle, WR logic to 0 to signal memory
- data enable (DEN) , is used to enable the data bus, DEN logic to 0 at is output

3. MINIMUM MODE

The **minimum mode** which is shown in figure (5). is selected by applying **logic 1** to the **MN/MX** input lead. It is typically used for smaller **single microprocessor** systems.

Summery of minimum mode interface signals:

- **Address/Data Bus:** The address bus is **20 bits long** and consists of signal lines **A0** (LSB) through **A19** (MSB). However, only address lines **A0** through **A15** are used when accessing **I/O**.
- The **data bus** lines are **multiplexed** with address lines. For this reason, they are denoted as **AD0** through **AD15**. Data line **D0** is the LSB.
- **Status Signals:** The four most significant address lines **A16** through **A19** of the 8086 are multiplexed with **status signals S3**

through **S6**. These status bits are output on the bus at the same time that data are transferred over the other bus lines.

Control Signals:

- When *Address latch enable* (**ALE**) is **logic 1** it signals that a **valid address** is on the bus. This address can be latched in external circuitry on the **1-to-0 edge** of the pulse at ALE.
- **M/IO** (*memory/IO*) tells external circuitry whether a memory or I/O transfer is taking place over the bus. **Logic 1** signals a **memory operation** and **logic 0** signals an **I/O operation**.
- **DT/R** (*data transmit/receive*) signals the **direction of data transfer** over the bus. **Logic 1** indicates that the bus is in the **transmit mode** (i.e., data are either written into memory or to an I/O device). **Logic 0** signals that the bus is in the **receive mode** (i.e., reading data from memory or from an input port).
- The *bank high enable* (**BHE**) signal is used as a **memory enable signal** for the **most significant byte** half of the data bus, **D8** through **D15**.
- **WR** (*write*) is switched to **logic 0** to signal external devices that **valid output data** are on the bus.
- **RD** (*read*) indicates that the MPU is performing a **read of data** off the bus. During read operations, one other control signal, **DEN** (*data enable*), is also supplied. It enables external devices to supply data to the microprocessor.
- The **READY** signal can be used to **insert wait states** into the bus cycle so that it is extended by a number of clock periods. This signal is supplied by a **slow memory or I/O subsystem** to signal the MPU when it is ready to permit the data transfer to be completed.
- **Interrupt Signals:**
 - *Interrupt request* (**INTR**) is an **input** to the 8086 that can be used by an **external device** to **signal** that it needs to be **served**. **Logic 1** at INTR represents an active interrupt request.
 - When the MPU **recognizes an interrupt request**, it indicates this fact to external circuits with logic 0 at the *interrupt acknowledge* (**INTA**) output.
 - On the **0-to-1 transition** of *nonmaskable interrupt* (**NMI**), control is passed to a nonmaskable **interrupt service routine** at completion of execution of the current instruction. NMI is the interrupt request with highest priority and **cannot be masked by software**.

- The **RESET** input is used to provide a **hardware reset** for the MPU. Switching RESET to **logic 0** initializes the internal registers of the MPU and initiates a reset service routine.

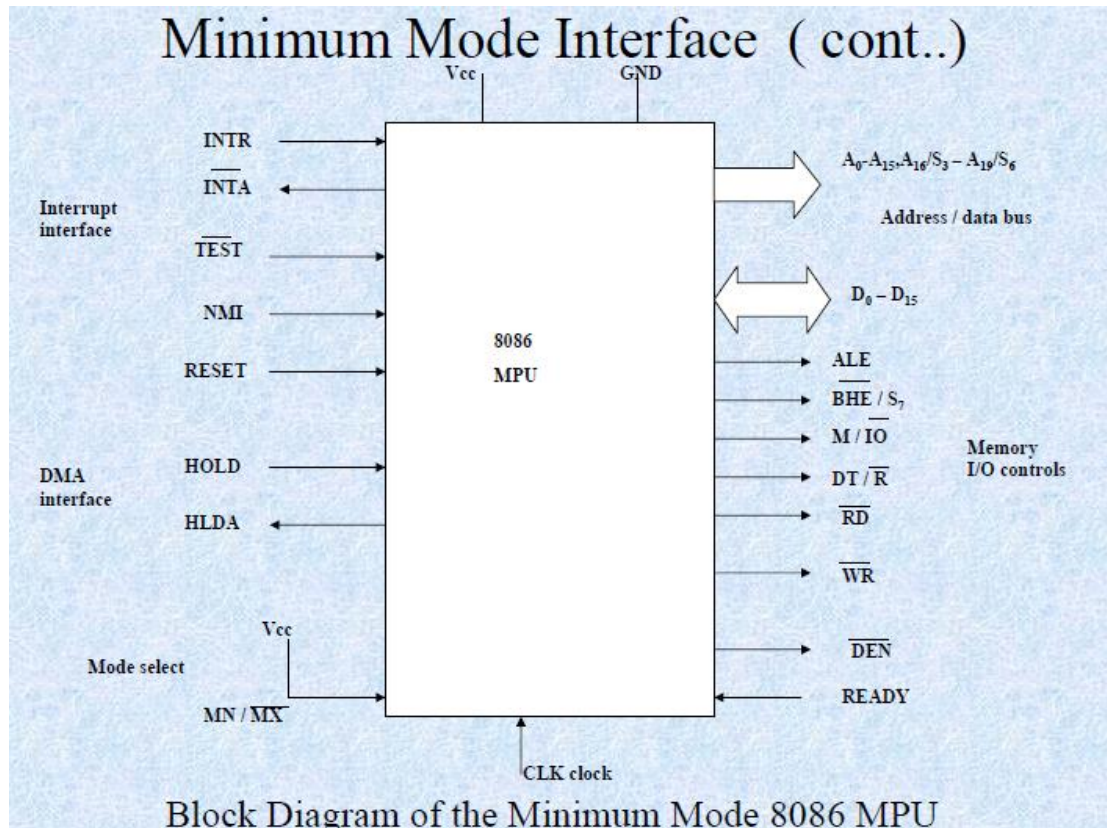


Figure 5: block diagram of the minimum mode

2.2 MEMORY READ AND WRITE BUS CYCLES

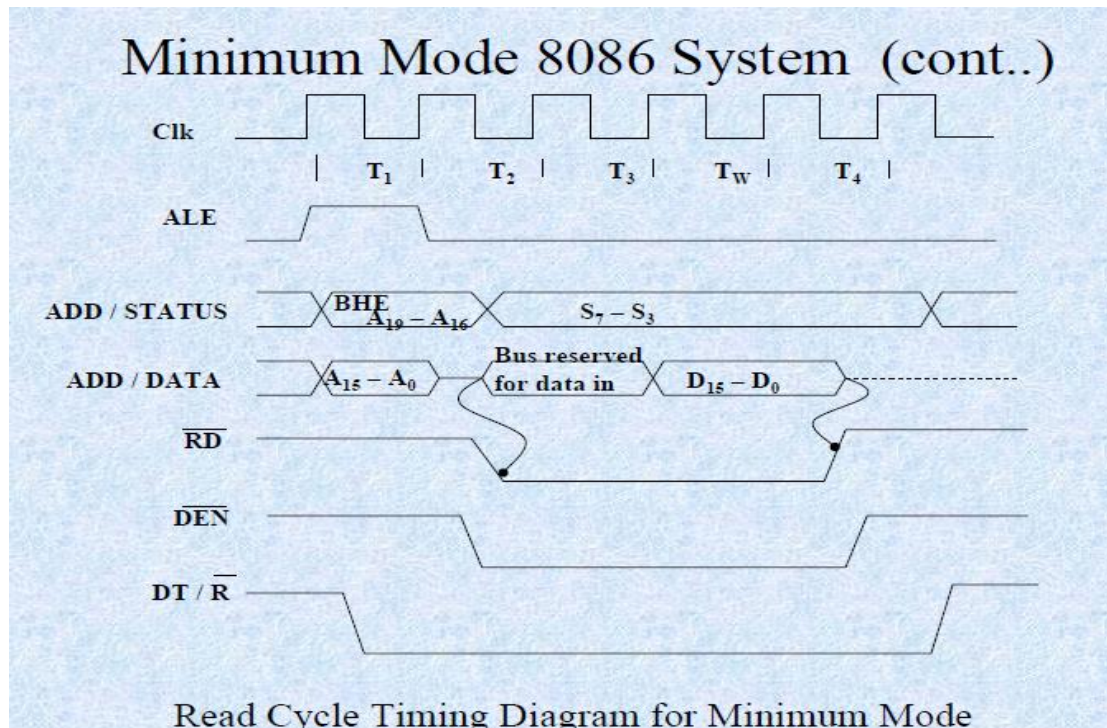
Memory read which shown in **Figure (6-a)** can describe as:

- During **period T1**,
 - The 8086 outputs the **20-bit address** of the memory location to be accessed on its multiplexed **address/data bus**. **BHE** is also output along with the address during T1.
 - At the same time a pulse is also produced at **ALE**. The **trailing edge** or the **high level** of this pulse is used to **latch** the address in external circuitry.
 - Signal **M/I0** is set to **logic 1** and signal **DT/R** is set to the **0 logic level** and both are maintained throughout all four periods of the bus cycle.
- Beginning with **period T2**,
 - Status bits **S3** through **S6** are output on the upper four address bus lines. This status information is maintained through periods **T3** and **T4**.

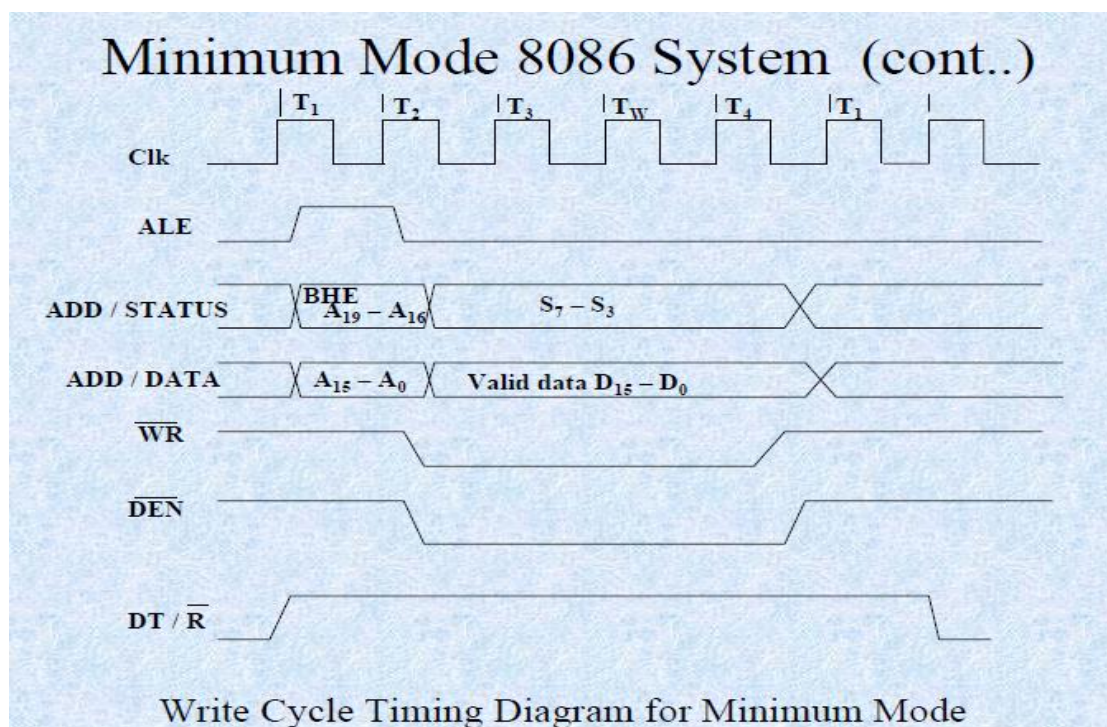
- On the other hand, address/data bus lines **AD0 through AD7** are put in the **high-Z state** during **T2**.
 - Late in period **T2**, **RD** is switched to **logic 0**. This indicates to the memory subsystem that a read cycle is in progress. **DEN** is switched to **logic 0** to enable external circuitry to allow the data to move from memory onto the microprocessor's data bus.
 - During **period T3**,
 - The memory must provide **valid data** during **T3** and maintain it until after -the processor terminates the read operation. The data read by the 8086 microprocessor can be carried over all **16 data bus lines**
 - During **T4**,
 - The 8086 switches **RD** to the inactive **1 logic level** to terminate the read operation. **DEN** returns to its inactive logic level late during **T4** to disable the external circuitry.
- a **memory write cycle** which shown in **Figure (6-b)** can describe as:

- During **period T1**,
 - The **address** along with **BHE** are output and latched with the **ALE** pulse.
 - **M/IO** is set to **logic 1** to indicate a memory cycle.
 - However, this time **DT/R** is switched to **logic 1**. This signals external circuits that the 8086 is going to **transmit data** over the bus.
- Beginning with **period T2**,
 - **WR** is switched to **logic 0** telling the memory subsystem that a write operation is to follow.
 - The 8086 puts the **data** on the bus late in **T2** and maintains the data valid through **T4**. Data will be carried over all **16 data bus lines**.
 - **DEN** enables the external circuitry to provide a path for data from the processor to the memory.
- During **period T3**,
 - The memory must receive **valid data** during **T3** and maintain it until after -the processor terminates the write operation. The data write by the 8086 microprocessor can be carried over all **16 data bus lines**
- During **T4**,

- The 8086 switches **WR** to the inactive **1** logic level to terminate the write operation. **DEN** returns to its inactive logic level late during **T4** to disable the external circuitry.



a-read cycle



b-write cycle

figure 6:minimum mode a-read cycle b-write cycle

4. MAXIMUM MODE

In the maximum mode, the 8086 is operated by strapping the MN/MX pin to ground. In this mode which shown in figure (7), the processor derives the status signal S₂, S₁, S₀ and Another chip called bus controller derives the control signal using this status information . In the maximum mode, there may be more than one microprocessor in the system configuration.

The basic function of the bus controller chip IC8288, is to derive control signals like RD and WR (for memory and I/O devices), DEN, DT/R, ALE etc. using the information by the processor on the status lines. The bus controller chip has input lines S₂, S₁, S₀ and CLK. These inputs to 8288 are driven by CPU. It derives the outputs ALE, DEN, DT/R, MRDC, MWTC, AMWC, IORC, IOWC and AIOWC. The AEN, IOB and CEN pins are specially useful for multiprocessor systems.

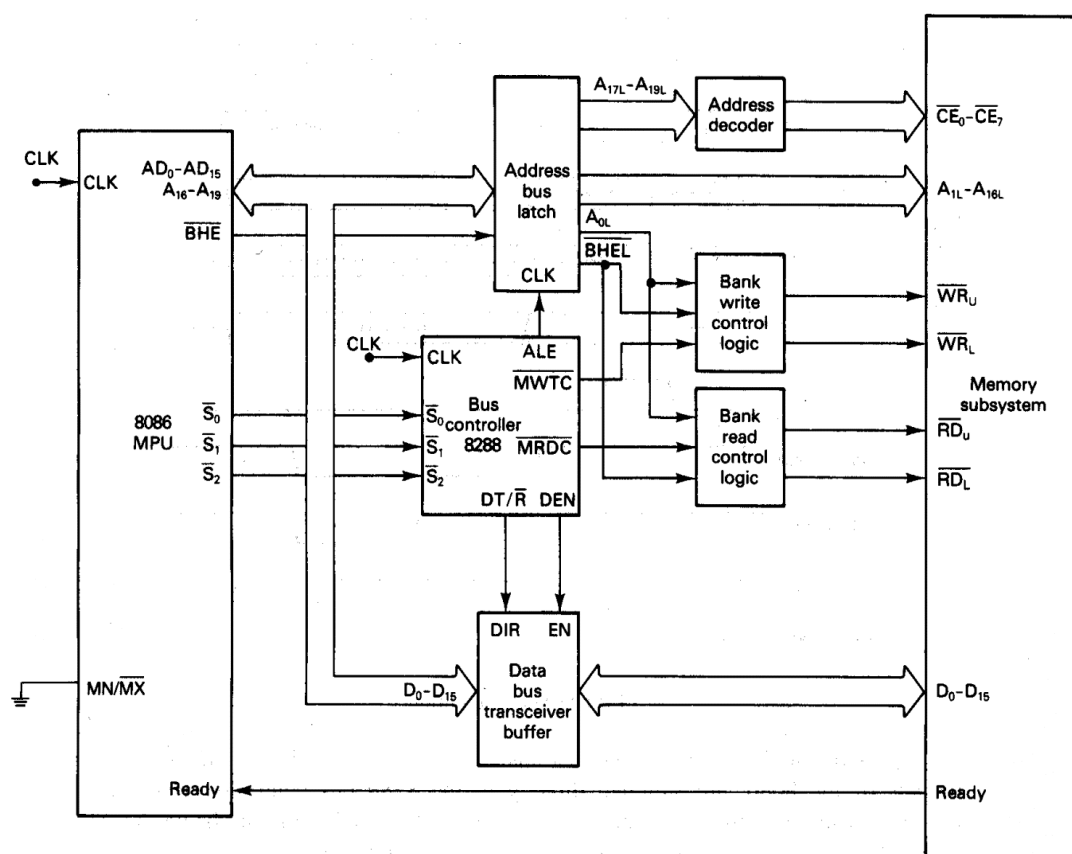


Figure 7:Maximum 8086 block diagram

The difference between in timing diagram between minimum mode and maximum mode is the status signals used and the available control and advanced command signals. S₀, S₁, S₂ are set at the beginning of bus cycle. The 8288 bus controller will output a pulse as on the ALE and

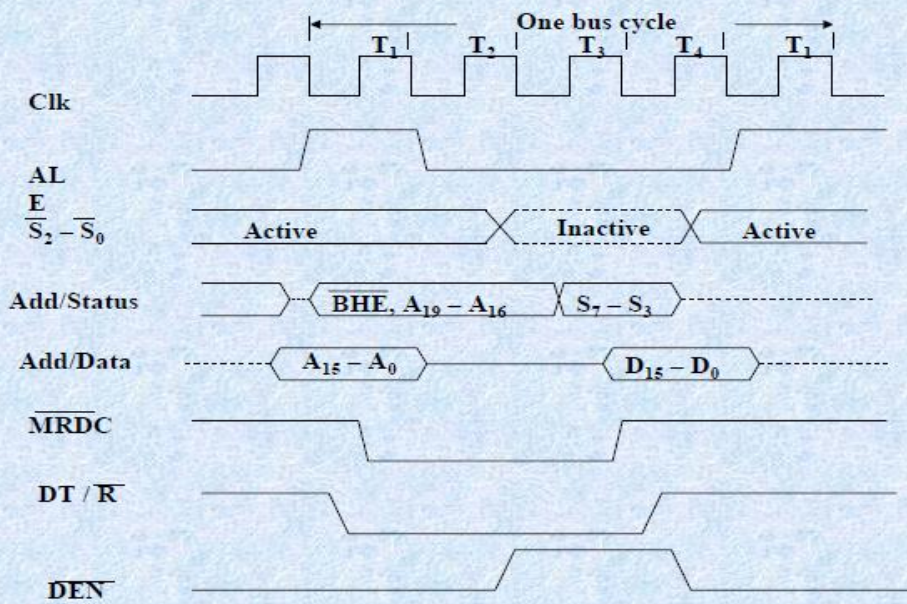
apply a required signal to its DT / R pin during T1. In T2, 8288 will set DEN=1 thus enabling transceivers, and for an input it will activate MRDC or IORC. These signals are activated until T4. For an output, the AMWC or AIOWC is activated from T2 to T4 and MWTC or IOWC is activated from T3 to T4. The status bit S0 to S2 remains active until T3 and become passive during T3 and T4 **and** If reader input is not activated before T3, wait state will be inserted between T3 and T4. Memory read and write cycles are shown in figure (8). Another signal output from microprocessor is queue status signal.

Queue Status Signals : Two new signals that are produced by the 8086 in the maximum-mode system are queue status outputs QS0 and QS1. Together they form a 2-bit queue status code, QS1QS0. • Following table shows the four different queue status.

Table :Queueing status table

QS ₁	QS ₀	Queue Status
0 (low)	0	No Operation. During the last clock cycle, nothing was taken from the queue.
0	1	First Byte. The byte taken from the queue was the first byte of the instruction.
1 (high)	0	Queue Empty. The queue has been reinitialized as a result of the execution of a transfer instruction.
1	1	Subsequent Byte. The byte taken from the queue was a subsequent byte of the instruction.

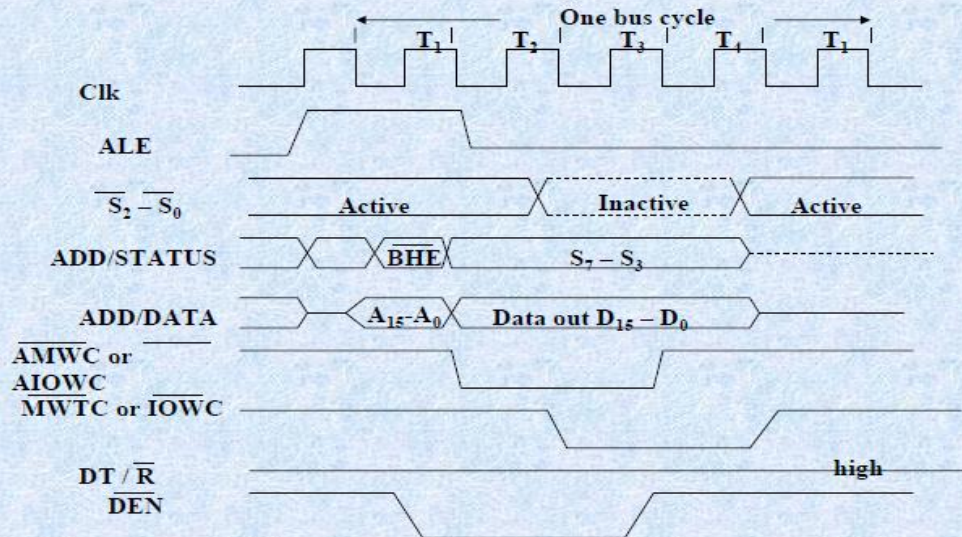
Maximum Mode 8086 System (cont..)



Memory Read Timing in Maximum Mode

a-memory read cycle

Maximum Mode 8086 System (cont..)



Memory Write Timing in Maximum mode.

b-memory write cycle

figure 8:maximum mode a-memory read cycle

b-memory write cycle