

DIODE TRANSISTOR LOGIC

Resistor-Transistor Logic was an early form of logic used in the 1950's and early 1960's. RTL was made from discrete transistors and resistors and manufactured on printed circuit boards with several gates per board. These boards were plugged into board sockets with wiring on the socket pins determining the system function. RTL was a big improvement over vacuum tube technology previously used, requiring less than one quarter the space and one tenth the power dissipation. RTL was superseded in the 1960's by Diode-Transistor Logic and then Transistor-Transistor Logic, DTL and TTL respectively. DTL was initially made with discrete transistors and resistors before being integrated onto silicon. One early form of DTL, used by IBM Corp in the 360 family of computers, was really a hybrid technology. Transistor and diode chips were glued to a ceramic substrate and aluminum resistor paste was deposited on the substrate to make resistors. Finally the ceramic base and components were hermetically sealed in an aluminum can. This family was used extensively in IBM products in the middle to late 1960's. While this family was not a true integrated circuit, it was very successful and was less expensive than true integrated circuits for several years. By the early 1970's integrated circuits became quite common and DTL gave way to TTL which was more appropriate to integrated circuit technology.

While DTL is no longer commercially used, we will discuss it because it is similar to and easier to understand than TTL, and because designers still find the configuration of value. First, however, we will discuss diode logic which is the front end of the DTL gate and performs the actual logic operation.

DIODE LOGIC

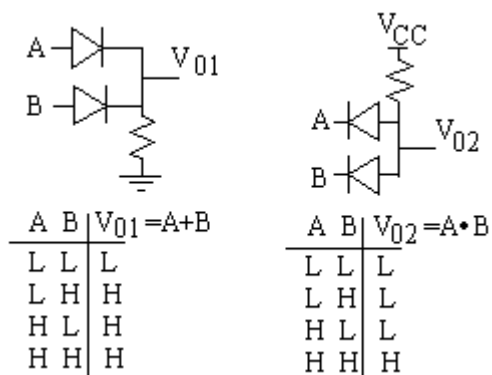


Figure 1. Diode logic and truth tables

Two diode logic configurations are shown in Figure 1. The truth tables show that the first circuit performs a logical OR and the second circuit performs a logical AND. One problem with these circuits is that there is a voltage level shift through the circuit. If several circuits are cascaded as shown in Figure 2, the output voltage for each stage is approximately one diode voltage drop further away from the rail. Logic "0" rises for the

AND gate and logic "1" drops for the OR gate. Only a limited number of series cascaded circuits can be used before the logic levels must be restored to the rails. Even more serious is the voltage degradation for the cascaded AND-OR function.

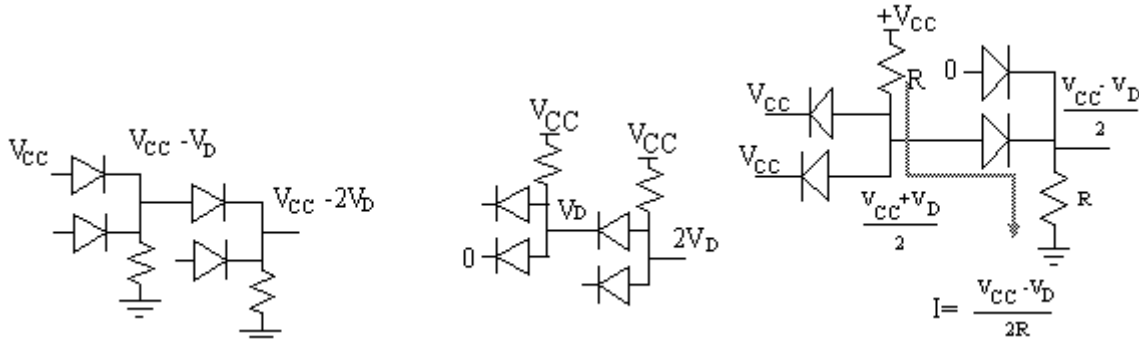


Figure 2. Cascaded diode logic showing level shifts.

The obvious way to restore the logic level voltages is to use a double transistor inverter. However, it does not take a genius to notice the a single inversion on the end of each gate will make a NAND or a NOR gate and the logic level is automatically restored for each gate. The NAND gate is used extensively. As you no doubt recall, any logic expression can be implemented using just NAND gates. Thus, other forms are not necessary.

DIODE TRANSISTOR LOGIC CIRCUITS

A typical DTL NAND gate is shown in Figure 3. Observe the diode AND function on the front end and the transistor NOT at the output end. The extra resistors and diodes are used to maintain appropriate currents, to maintain proper functioning, and to guarantee certain noise margins. We will completely analyze this circuit, but will be particularly interested in the "terminal" characteristics of the gate. Our ultimate goal is to understand the operation of the gate so that the manufacturer's specifications can be understood.

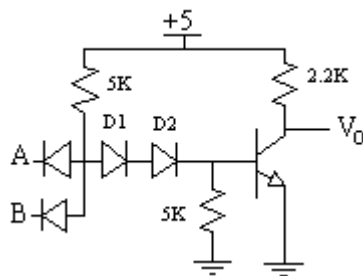


Figure 3. DTL Circuit

ANALYSIS OF THE DTL GATE

Analysis of the DTL gate is dependent on complete understanding of the currents within the gate under all logic conditions. First let us develop a generic understanding of the operation. *Of particular importance will be the direction of currents at the terminals of the gate.* As in most logic systems, the transistor will either be cutoff or saturated.

If all inputs are high, (+5v), no current will come out of the input diodes at the input and current will flow down through the first 5K resistor and through the diodes D1 and D2 toward the base of the transistor. Some current will split off and go down through the lower 5K resistor to ground. However, most of the current will go into the base of the transistor causing it to saturate, pulling the output low, $V_O = 0.2$ Volts. We will show this condition quantitatively shortly.

If one or more of the inputs to the gate are held low (0.2 V), then the current down through the 5K resistor will go out the input diode, away from the transistor base. Under this condition, the transistor will be cutoff and the output will be high with $V_O = 5$ Volts.

ANALYSIS WITH INPUT LOW

Quantitatively, we will start with one or more inputs held low, at 0.2 Volts. From the logic function of the NAND gate, we know that the output is supposed to be high. Therefore, the transistor must be cutoff. To begin with, we will assume the two diodes D1 and D2 in series will also be cutoff. All the current coming down through the 5K resistor must all go out through the input diode, causing it to be on. The circuit with the models indicated is shown in Figure 4. From this circuit we can calculate all voltages and currents and prove (or disprove) our assumptions about the condition of each element.

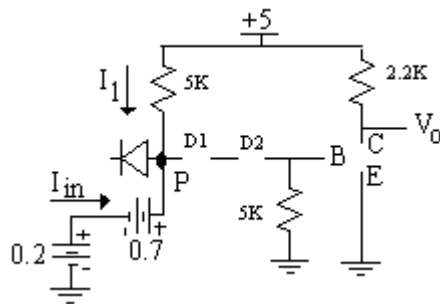


Figure 4. DTL gate model with input low

The voltage at point P is

$$V_P = 0.2 + 0.70 = 0.90 \text{ Volts.}$$

We need to show that this voltage is low enough that the two series diodes and the transistor will be cutoff. The argument is that if either diode carries current, then both must. Since 0.9 Volts is not enough across the pair to maintain conduction, then neither conducts. Given that the diodes are off, then the voltage at the base of the transistor is zero, and is also cutoff. We can verify that the input diode is conducting by observing that current I_1 is

$$I_1 = (5-0.9)/5K = 0.82 \text{ mA}$$

This current leaves through the input diode, hence it is on. The current entering the input terminal is

$$I_{in} = -I_1 = -0.82 \text{ mA}$$

The negative sign occurs because the input current is defined as going into the terminal.

We can now verify that the output voltage is 5 Volts because the transistor has been shown to be cutoff. Thus,

$$V_O = 5.0 \text{ Volts}$$

One other characteristic of the DTL gate that can be obtained at this point is the range of input voltages that will be recognized as a "low". From the logic function of the NAND gate, this can be translated into the question of how high the input voltage may rise and still keep the transistor cutoff.

The transistor will remain cutoff as long as the voltage at the base does not rise above 0.5 volts. At this voltage, there will be current down through the lower 5K resistor to ground. This current must come from the +5 supply down through the upper 5K resistor and the diodes, D1 and D2. Hence the diodes must be conducting. This current will be 0.1 mA. The voltage at point P will be

$$V_P = 0.5 + 0.7 + 0.7 = 1.9 \text{ Volts}$$

The current I_1 is

$$I_1 = (5-1.9)/5K = 0.62 \text{ mA}$$

The current going out through the input diode will be

$$I_{in} = -(0.62 - 0.1) = -0.52 \text{ mA}$$

indicating that the input diode is still conducting. Figure 5 shows the resulting circuit with the circuit models included. The maximum voltage at the input that is guaranteed to be recognized as a low is

$$V_{inLmax} = 1.9 - 0.7 = 1.2 \text{ Volts.}$$

This result is included in the table of terminal specification at the end of this chapter.

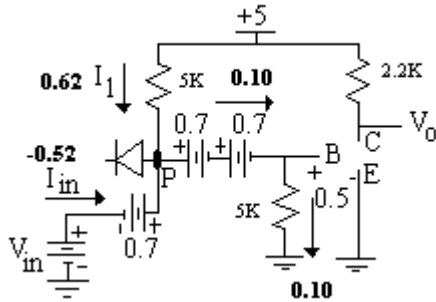


Figure 5. DTL circuit model with $V_{in} = V_{inLmax}$

ANALYSIS WITH ALL INPUTS HIGH

When all inputs are high, all current down through the upper 5K resistor will go toward the base of the transistor, causing it to saturate. The series diodes will obviously be conducting, and we will show that the input diodes are cutoff. Figure 6 shows the circuit with these models.

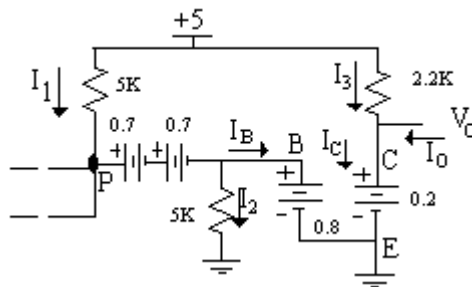


Figure 6. DTL circuit model with inputs high

The voltage at point P is

$$V_P = 0.8 + 0.7 + 0.7 = 2.2 \text{ volts}$$

Thus, I_1 is

$$I_1 = (5 - 2.2) / 5K = 0.56 \text{ mA}$$

This current will go through the diodes toward the base of the transistor. Some of the current will go down through the lower 5K resistor with the rest going into the base of the transistor. With the transistor saturated, the current going down through the 5K resistor will be

$$I_2 = 0.8 / 5K = 0.16 \text{ mA}$$

The base current then is

$$I_B = 0.56 - 0.16 = 0.4 \text{ mA}$$

If the transistor is to be saturated, the maximum collector current is

$$I_{Cmax} = \beta I_B = 30 * 0.4 \text{ mA} = 12.00 \text{ mA}$$

at saturation, the current coming down through the 2.2K collector resistor is

$$I_3 = (5-0.2)/2.2K = 2.182 \text{ mA}$$

this current is much less than the maximum saturation current and we see that with no load, the transistor will, indeed, be in saturation. In fact, there is excess capacity in collector saturation current. This excess capacity can be used to **sink** external load current. This current is called I_o or load current. The maximum load current this gate can sink is

$$I_{oLmax} = 12.00 \text{ mA} - 2.182 \text{ mA} = 9.818 \text{ mA}$$

Note that this current is entering the terminal of the gate, hence, is positive.

CALCULATION OF V_{inHmin} and I_{inH}

We need to go back now and look at the input voltage in Figure 6 and determine the minimum allowable input voltage that will still be recognized as a high, V_{inHmin} . There are several ways we could define this value, but we will use a straightforward definition. That is, we will define the input to be high as long as no current flows through the input diodes. In other words, as long as the input diodes are cutoff. Thus,

$$V_{inHmin} = V_P - 0.60 = 2.20 - 0.60 = 1.6 \text{ Volts.}$$

Since the input diodes must remain cutoff, $I_{inH} = 0$.

CALCULATION OF FANOUT

If several load gates are connected to the output terminal of the gate we are looking at, we need to look at the current output drive capability compared to the input current requirements of the load gates. Because the input current is zero when high, an infinite number of load gates can be driven when high. However, the DTL gate requires current when the input is low. This situation is shown in Figure 7. We made that calculation earlier and found $I_{inLmax} = - 0.82 \text{ mA}$. Note that this current is negative meaning that it is coming out of the input terminal. We also found the output of a gate can sink 9.818 mA when it is low. We can now calculate the fanout.

$$Fanout \leq \frac{I_{oLmax}}{I_{inL}} = \frac{9.818}{0.82} = 11.97$$

The maximum number of gates that can be driven as loads is 11.

$$Fanout = 11$$

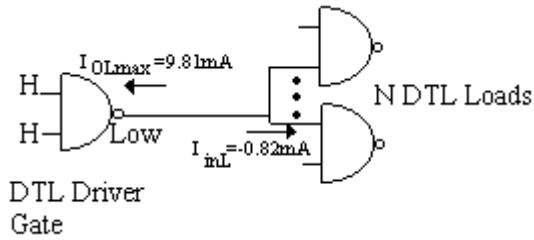


Figure 7. DTL driver gate with N identical DTL load gates

We also need to check voltage compatibility. That is, $V_{oH} > V_{inHmin}$ and $V_{oL} < V_{inLmax}$ which is true as shown in Figure 8 where V_{oH} is given at no load condition because $I_{inH} = 0$.

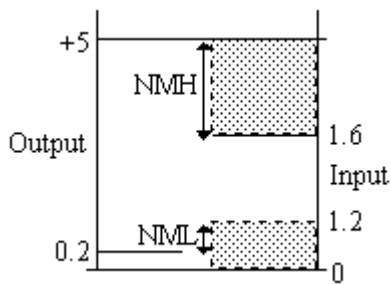


Figure 8. Comparison of output and input voltages for DTL gate.

CALCULATION OF V_{oH} AND I_{oH}

We now have calculated all terminal characteristics except for the output voltage and current when the output is high. Because $I_{inH} = 0$, with any number of loads there will be zero load current. Thus, $V_{oH} = 5.0$ Volts. This specification is satisfactory if the only load is other gates. In many cases, however, we wish to use other types of loads and additional information is necessary.

When the output is high, the transistor is cutoff and any current coming out of the gate will come from the supply through the collector resistor. One way to define the output is when the output is allowed to drop as low as V_{inHmin} (although this is by no means the only way). Using this definition, we can calculate the output current as

$$I_{oH} = -(5-1.6)/2.2K = -1.545 \text{ mA}$$

Again, the negative sign indicates that current flows out.

We now have a complete set of specifications for the DTL gate as shown in Table 1.

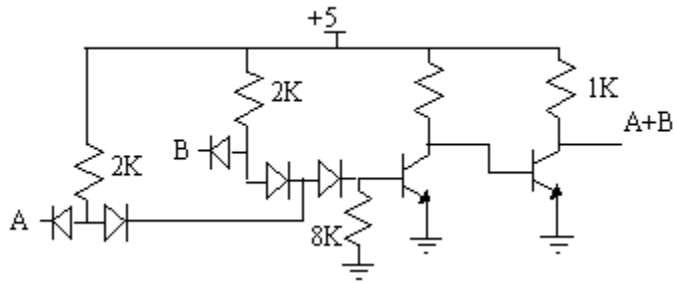


Figure 11. DTL OR gate

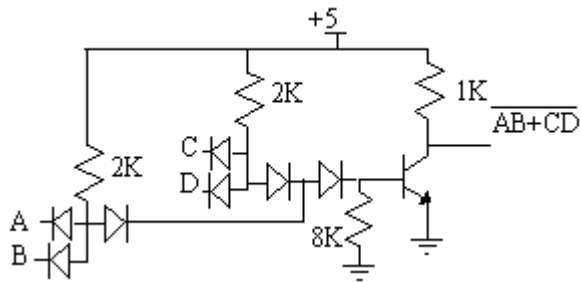
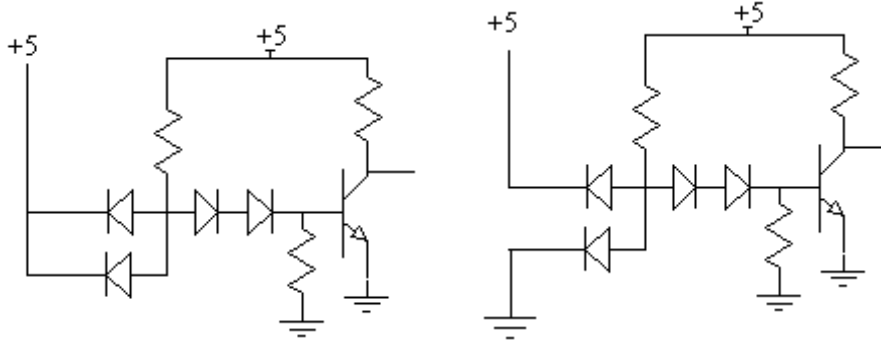


Figure 12 DTL AND-OR-INVERT gate

EXERCISES

1. For the following two DTL gate circuits as shown:
 - a. Write the logic levels (H or L) at both inputs and the output.
 - b. What is the state of the transistor?
 - c. Draw arrows showing the direction of all currents in the circuit.



For the following exercises, the manufacturer of DTL gates gives the following specifications:

$$V_{inLmax} = 1.00 \text{ Volts}$$

$$V_{oLmax} = 0.30 \text{ volts}$$

$$V_{inHmin} = 2.00 \text{ volts}$$

$$V_{oHmin} = 2.75 \text{ volts}$$

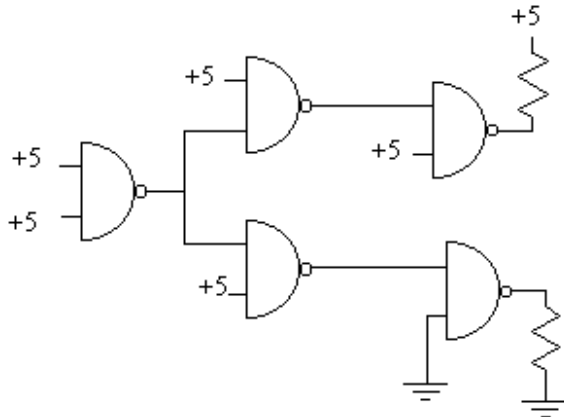
$$I_{inLmax} = -1.00 \text{ mA}$$

$$I_{oLmax} = 10.00 \text{ mA}$$

$$I_{inH} = 0.00$$

$$I_{oHmax} = -5.00 \text{ mA (@} V_o = 2.75 \text{ v)}$$

3. A logic system shown below is made up of DTL gates.
 1. Write the logic level (H or L) beside each input and output for each gate.
 2. Draw arrows beside each connecting wire, including inputs and outputs, showing the direction of current in the wire. If zero, write I=0.



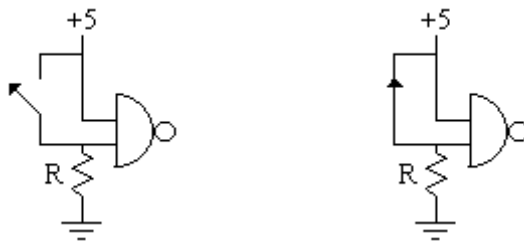
4. On the diagram, give the magnitude of all currents except the two final outputs.

5. Determine the minimum value of each of the load resistors if the gates are to be operated within specifications and logic levels are preserved.

$$R_{\text{pullup min}} = \underline{\hspace{2cm}} \qquad R_{\text{pulldown min}} = \underline{\hspace{2cm}}$$

6. The circuit below is used to interface a switch to the DTL gate specified above. It is assumed that with the switch in one position, the gate sees a valid logic low, and when the switch is in the other position, the gate sees a valid logic high.

- a. Indicate on the drawings, which logic level the gate input sees.
- b. Draw arrows showing currents when the switch is open and when the switch is closed.



7. For the input interface circuit above, determine the maximum value of R that can be used and still have the gate operate within specifications. What determines the minimum value of R?

$$R_{\text{max}} = \underline{\hspace{2cm}}$$

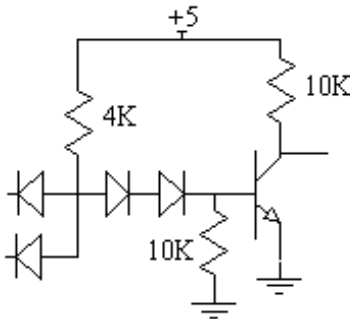
R_{min} is determined by:

Problems

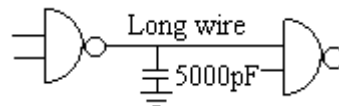
1. Your employer, Mountaineer Logic, Inc., is developing a new line of discrete DTL gates shown below. Write up a specification sheet for the device. (Use nominal calculations only.) Define the high level output current at $V_O = V_{inHmin} + 1.0$ volts. Use a tabular format similar to the DTL data sheet given in this chapter. Assume the following diode and transistor models.

$$V_{Dcutin} = 0.6, V_{Don} = 0.7, V_{BEcutin} = 0.5, V_{BESat} = 0.8, \text{Beta} = 20$$

2. The Quality Control Department of MLI just called you about the DTL gate above. It seems they connected it to a network with a single load gate. The output rise time seemed much too long. Upon questioning, you discover that they used a very long wire to connect between the driver and the load. You estimate that the capacitance of the wire to be 5000 pF as shown in the figure below. Estimate how long it will take to charge the capacitor so the output of the gate to rise from a "low" to V_{inHmin} . Because you are a professional, present only the circuit you used, the results, and the assumptions you made (including circuit models). Do not show details of the calculations.



DTL Gate



Circuit with 5000pF capacitive load

3. The manufacturer's specifications for a DTL gate are:

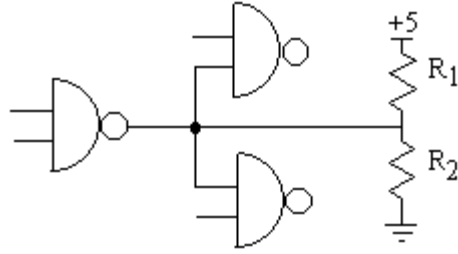
$$V_{inLmax} = 1.00 \text{ volts} \quad V_{oLmax} = 0.30 \text{ volts}$$

$$V_{inHmin} = 2.00 \text{ volts} \quad V_{oHmin} = 2.75 \text{ volts}$$

$$I_{inLmax} = -1.00 \text{ mA} \quad I_{oLmax} = 10.00 \text{ mA}$$

$$I_{inH} = 0.00 \quad I_{oHmax} = -5.00 \text{ mA} (@V_O = 2.75 \text{ v})$$

This gate is used to drive two identical gates, plus a resistive load as shown. Determine the allowed range for R_1 if $R_2 = 2200$ Ohms.



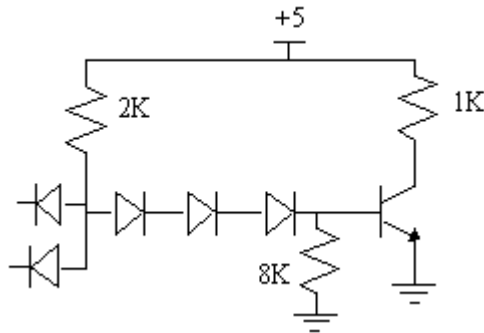
4. A DTL gate has an additional diode added as seen in the circuit below. Determine V_{inLmax} , V_{inHmin} , I_{inL} , I_{inH} , and I_{oLmax} .

Diode Models:

$$V_{D\gamma} = 0.60, \quad V_{Don} = 0.70 \text{ volts}$$

Transistor Models:

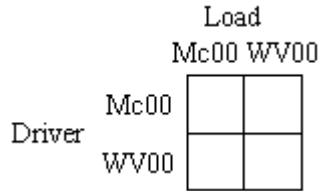
$$V_{BE\gamma} = 0.50, \quad V_{BEsat} = 0.80, \quad V_{CEsat} = 0.20, \quad \text{Beta} = 20$$



6. Two logic families are being used in a logic system. Their terminal specifications are given below. Fill in the compatibility chart.

	Mc00	WV00
V_{inLmax}	1.00	1.50
V_{inHmin}	2.00	3.00
I_{inL}	- 0.500	- 1.00 mA
I_{inH}	1.00	0.050 mA
V_{oLmax}	0.50	0.75

V_{oHmin}	2.50	4.00
I_{oLmax}	5.50	8.00 mA
I_{oHmax}	-7.00	-2.50 mA



7. In the following logic circuit, all the gates are Mc00 gates whose specifications are given below. Determine the range of resistance allowed for the resistor R such that all gates are working within their specifications. Note that the load gates must see a legitimate logic low and legitimate logic high.

$$V_{inLmax} = 1.00 \quad V_{inHmin} = 2.00 \quad I_{inL} = -0.500 \quad I_{inH} = 1.00$$

$$V_{oLmax} = 0.50 \quad V_{oHmin} = 2.50 \quad I_{oLmax} = 5.50 \quad I_{oHmax} = -7.00$$

