TRANSISTOR-TRANSISTOR LOGIC

The evolution from DTL to TTL can be seen by observing the placement of p-n junctions. For example, the diode D2 from Figure 2 in the chapter on DTL can be replaced by a transistor whose collector is pulled up to the power supply; transistor Q2 in Figure 1 below. The p-n junction of D2 is replaced by the BE junction of Q2 and with the current gain of the transistor, the current going into the base of Q3 is greatly increased, increasing the fanout.

The input diodes and D1 are replaced by the multi-emitter NPN transistor, Q1, in Fig. 1 and represented by the drawing in Figure 2. Later on, we will make additional modifications to this circuit to improve its performance further.

The analysis of this circuit follows very much the same path as the analysis of the DTL gate. For the most part, we will consider the input transistor, Q1, to act just like two diodes. The transistor Q2, however, will operate in all three regions. The treatment of the output voltages and currents will be treated the same as the DTL gate and Q3 will either be cutoff or saturated, corresponding to an output high and an output low, respectively.

ANALYSIS WITH ONE OR MORE INPUTS LOW

With an input low, Q3 should be cutoff. We will assume Q2 is cutoff and then check our assumption. If Q2 is cutoff, then there can be no current coming out of the collector of Q1, hence its base-collector junction can be modeled as an open circuit. The base-emitter junction of Q1 will be conducting. The circuit with these models substituted for the transistors is shown in Figure 3. Note the similarity to the DTL circuit under the same conditions. The two unused inputs are assumed to be high, and are thus, modeled as open. From this case, we can see that $V_{oh} = 5$ volts with no load, and

$$I_{inL} = -I_1 = -(5-0.9)/4K = -1.025 \text{ mA}$$
We turn now to finding $V_{\text{inLmax}}$. We will use the criterion that $V_{\text{in}}$ will be considered as a low as long as Q3 is kept cutoff. If the base voltage for Q3 can be raised to 0.5 Volts without turning it on, then there will be 0.5 mA current in the 1K\(\Omega\) resistor. This current can only come from Q2, which means it must be conducting. Even assuming all this 0.5 mA comes through the collector of Q2, the voltage drop across the 1.4 K\(\Omega\) resistor will be 0.7 Volts, not enough to cause the transistor to saturate. Thus, the active model for Q2 is appropriate as shown in Figure 4.

If we assume that $\beta=30$, the base current in Q2 is

$$I_{b2} = \frac{0.5\text{mA}}{\beta + 1} = \frac{0.5}{31} = 0.016\text{mA}$$

Because this current is coming out of the collector of Q1, the base-collector junction of Q1 is on, and is modeled as a diode in Figure 4.

The voltage at B1, the base of Q1, is

$$V_{B1} = 0.5 + 0.7 + 0.7 = 1.9\text{ Volts}$$

The current coming down through the 4 K\(\Omega\) resistor, $I_1$, is

$$I_1 = \frac{5.0 - 1.9}{4K} = 0.775\text{mA}$$

This is considerably more than is going into the base of Q2, therefore, the input BE junction of Q1 will also still be conducting. The maximum voltage at the input is

$$V_{\text{inLmax}} = 1.9 - 0.7 = 1.2\text{ Volts}$$
CALCULATIONS WITH INPUT HIGH

The circuit model for the TTL gate with all inputs high is shown in Figure 5. Both Q2 and Q3 are modeled as saturated, an assumption that must be verified. With the inputs high, Q1 is modeled as two diodes with the B-E diodes cutoff, and B-C diode conducting.

![TTL gate circuit model with all inputs high.](image)

Figure 5. TTL gate circuit model with all inputs high.

The voltage at the base of Q1 is

\[ V_{B1} = 0.8 + 0.8 + 0.7 = 2.3 \text{ Volts.} \]

The current down through the 4 KΩ resistor, \( I_1 \) is

\[ I_1 = \frac{5.0 - 2.3}{4K} = 0.675mA \]

All this current goes into the base of Q2.

\[ I_{B2} = 0.675 \text{ mA} \]

If Q2 is saturated, voltage at its collector terminal is

\[ V_{C2} = 0.8 + 0.2 = 1.0 \text{ Volts} \]

And the collector current is

\[ I_{C2} = I_2 = \frac{5.0 - 1.0}{1.4K} = 2.857mA \]

Clearly, if \( \beta = 30, \beta I_{B2} > I_{C2} \), and, therefore, Q2 is saturated.

The current coming out of the emitter of Q2 is the sum of the base and collector currents. Part of this current will go down through the 1 KΩ resistor to ground and the rest will enter the base of Q3.

\[ I_{B3} = I_{B2} + I_{C2} - I_3 = 0.675 + 2.857 - 0.8 = 2.732 \text{ mA} \]
The maximum collector current that Q3 can carry and still be in saturation is $\beta I_{\text{B3}} = 81.96$ mA, assuming $\beta = 30$. The maximum current the gate can sink when the output is low

$$I_{\text{OLmax}} = I_{\text{Csatmax}} - I_4 = 81.96 - 1.2 = 80.76 \text{ mA}$$

Now let’s turn our attention back to the input and determine $V_{\text{inHmin}}$ and $I_{\text{inH}}$. We will define the input voltage to be high as long as no current goes out the input terminal. Thus, all we have to do is keep the input voltage high enough so that the B-E p-n junction of Q1 does not turn on. Thus,

$$V_{\text{inHmin}} = 2.3 - 0.6 = 1.7 \text{ Volts}$$

CALCULATION OF $I_{\text{inH}}$

With the input voltage at a high, say 5 volts, the transistor Q1 will be operating in the reverse active mode. The B-E junction is reverse biased, and the B-C junction is forward biased with a base current of 0.675 mA. If there were significant current gain, you would expect to see a large current going into the input. However, the reverse $\beta$ is typically on the order of 0.02. Thus,

$$I_{\text{inH}} = \beta R * I = 0.02 * 0.675 = 0.0135 \text{ mA}$$

This current would add to the current going into the base of Q2, but is ignored because it is quite small and because $\beta R$ is made as small as possible and this input current is a maximum and cannot be counted on.

THE TOTEM POLE OUTPUT STAGE

One of the problems with the TTL gate circuit we have been analyzing is that the pull-up resistor on the output transistor will prevent rapid charging of any wiring capacitance on the output. One way to improve the rise time is to reduce the resistance value as is often done, but this also increases the power dissipation when the output is low.

If we look at the circuit, we observe that when the transistor is saturated, it presents a very low effective resistance to ground. The problem arises when the output is high and the pull-up resistor is too large. Ideally we would like to have a very low resistance pull-up when the output is high, but a very high pull-up resistance when the output is low. In this way, we could get quick charging and very low power dissipation. The totem-pole output stage for TTL, shown in Figure 6, does just that.

![Figure 6. TTL gate with totem-pole output.](image)
This circuit operates just like the original circuit except that Q₄ is on when the output is high and off when the output is low. We need to verify this operation.

OUTPUT LOW

Figure 7 shows the TTL circuit with all inputs high and the output low. The models for the transistors are shown as before, except diode D and transistor Q₄ are added and shown as cutoff.

![Figure 7. TTL gate with totem-pole output circuit model with inputs high.](image)

The analysis of this circuit proceeds exactly the same as before. The currents, I₁, I₂, I₃, and I₃B are the same as before. With the diode and Q₄ not conducting, IoLmax is now the same as IC₄max, 81.96 mA. We only need to show that the diode D and transistor Q₄ are indeed off.

The voltage at the bottom of the diode is 0.2 Volts and the voltage at the base of Q₄ equal to the voltage at the collector of Q₂; Vc₂ = (0.2 + 0.8) = 1.0 Volts. Thus, the voltage across the B-E junction of Q₄ plus the diode is 0.8 Volts. If one conducts, the other must also. To take both out of cutoff would require at least 0.5 + 0.6 = 1.1 Volts. Thus, both are off.

OUTPUT HIGH

This condition occurs when one or more inputs are low. The circuit is shown in Figure 8 with the appropriate models used for the transistors and the diode. In this case, Q₂ and Q₃ are both cutoff while Q₄ and the diode are conducting. We have to assume here that there is some load and that the output current is not zero.
The current coming out the output terminal $I_S (=-I_o)$ is the sum of the currents coming down through the base and the collector. Thus,

$$I_S = I_{B4} + \beta I_{B4}$$

Because each TTL load represents 13 $\mu$A, if we assume there are 10 loads, then $I_S = 130$ $\mu$A. The base current is

$$I_{B4} = \frac{130 \mu A}{1 + \beta} = 4.2 \mu A$$

where we have assumed a $\beta$ of 30. Then taking the path down through the 1.4 K$\Omega$ resistor to the output, the output voltage is

$$V_o = 5.0 - 4.2 \mu A \cdot 1.4 K - 0.7 - 0.7 = 3.6 \text{ Volts}$$

The voltage drop across the 1.4 K$\Omega$ resistor is negligible. Of course as the current increases, the output voltage will drop further.

**TERMINAL SPECIFICATIONS OF THE TTL GATE**

We are now ready to make the table showing the terminal specifications for the TTL gate. These are shown in Table 1.

<table>
<thead>
<tr>
<th>$V_{inL_{max}}$</th>
<th>$V_{oL}$</th>
<th>$V_{inH_{min}}$</th>
<th>$V_{oH}$</th>
<th>$I_{inL}$</th>
<th>$I_{oL_{max}}$</th>
<th>$I_{inH}$</th>
<th>$I_{oH}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2 V</td>
<td>0.2</td>
<td>1.7</td>
<td>3.4 (@$I_o = -130$ $\mu$A)</td>
<td>-1.025 mA</td>
<td>81.96 mA</td>
<td>13 $\mu$A</td>
<td>undetermined</td>
</tr>
</tbody>
</table>
### TTL DATA

#### Recommended Operating Conditions

<table>
<thead>
<tr>
<th></th>
<th>74</th>
<th>74H</th>
<th>74L</th>
<th>74LS</th>
<th>74S</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CEO}$</td>
<td>4.75 - 5.25</td>
<td>4.75 - 5.25</td>
<td>4.75 - 5.25</td>
<td>4.75 - 5.25</td>
<td>4.75 - 5.25</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>400</td>
<td>50</td>
<td>200</td>
<td>400</td>
<td>1000</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>16</td>
<td>20</td>
<td>3.6</td>
<td>8</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>Operating Free-Air Temperature Range</td>
<td>0 - 70</td>
<td>0 - 70</td>
<td>0 - 70</td>
<td>0 - 70</td>
<td>0 - 70</td>
<td>°C</td>
</tr>
</tbody>
</table>

#### Electrical Characteristics Over Recommended Operating Temperature Range

<table>
<thead>
<tr>
<th>Condition</th>
<th>74</th>
<th>74H</th>
<th>74L</th>
<th>74LS</th>
<th>74S</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{max}$</td>
<td>2.00</td>
<td>2.00</td>
<td>2.00</td>
<td>2.00</td>
<td>2.00</td>
<td>V</td>
</tr>
<tr>
<td>$V_{min}$</td>
<td>0.80</td>
<td>0.80</td>
<td>0.70</td>
<td>0.80</td>
<td>0.80</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DSS}$</td>
<td>2.40</td>
<td>2.40</td>
<td>2.40</td>
<td>2.70</td>
<td>2.70</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>0.40</td>
<td>0.40</td>
<td>0.40</td>
<td>0.5</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{CBO}$</td>
<td>40</td>
<td>50</td>
<td>1.0</td>
<td>20</td>
<td>50</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{CEO}$</td>
<td>1.00</td>
<td>2.00</td>
<td>0.18</td>
<td>0.40</td>
<td>2.00</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CS}$</td>
<td>0.10</td>
<td>0.10</td>
<td>0.15</td>
<td>0.10</td>
<td>0.10</td>
<td>mA</td>
</tr>
</tbody>
</table>

* Not more than one output should be shorted at a time and for H, LS, and S series, duration of short should not exceed one second.

Figure 9. Data for ‘00, ‘04, ‘10, and ‘30 NAND gates for several TTL families (Abstracted from Texas Instruments TTL Data Book.)
MANUFACTURER’S DATA SHEETS

The terminal specifications of several TTL families are shown in Figure 9. You will note the values given for various voltages and currents are quite different from those we calculated. This difference comes from the fact that manufacturing tolerances and variations cannot be closely controlled, hence, the specifications given by the manufacturers are much more conservative than our calculations which were based on nominal values. Also note that the limits are usually given as a maximum or a minimum, depending on which limit is normally used in design. For example, $I_{\text{inLmax}}$ is given as -1.6 mA for the 74xx series. What this means is that as a designer, your driver must be able to sink as much as 1.6 mA when the input to the gate is pulled low.

You will note that the TTL gate is rather loosely specified. The question invariably arises as to how one reads the data sheets or designs with this data. Figure 10 shows the allowed operating regions for a 7400, 2-input NAND gate. The best description of these operating regions is probably given by the following examples.

Example 1: If the input voltage is between 0.00 and 0.08 volts, the output voltage will be below $V_{\text{CC}}$ and above 2.4 volts as shown in Figure 10a.

Example 2: If the input voltage is between 2.00 and $V_{\text{CC}}$, the input current will be between 0 and 40 $\mu$A as shown in Figure 10b.

You will note in the above examples that there is no mathematical relationship between one variable and another. There is simply not enough data to develop one and the variability of the manufacturing process prohibits the manufacturer from providing one.

In a design setting, you must stay within the limits provided by the manufacturer. For example, if you wanted to connect a resistor from the output of a 7400 gate and ground, what would be the limits allowed on the resistance value? Figure 10c provides part of the answer. If we assume that we must operate within the shaded region which represents a “High” level output, we should not allow the output to drop below 2.4 volts with 400 $\mu$A coming out of the gate. The minimum value would be 6 K$\Omega$. The upper limit is, of course, infinite; an open circuit ($V_o = V_{\text{CC}}, I_o = 0$).

There are a few data points provide by the specifications that are not within the limits of normal operation. For example, if the input voltage drops below zero, it is allowed to drop to -1.5 volts where you may expect as much as 12 mA coming out of a 7400 gate input. Most of this current comes from an input clamp diode which has not been shown on our drawings.
Figure 10. Allowed operating regions for a 7400 gate
Another non-standard data point of interest is $I_{OS}$, the short-circuit output current. This is the current you get from the gate output if the output is shorted to ground when the output of the gate would otherwise be high. In this case, both minimum and maximum values are given, -18 to -55 mA. If you went to the laboratory and actually performed this deed, you could expect a current somewhere in this range. How does this affect the designer? For example, a designer might be tempted to connect the output of the 7400 gate directly to the base of an NPN transistor whose emitter is grounded. In this case, the "high" output voltage is clamped at 0.80 V by the BE junction. What current can you expect into the base of the transistor when the gate output goes "high"? This condition is tricky and perhaps open to some debate, but the conservative designer must recognize that the operation is between the short circuit case and the case where $V_{OH\text{min}}=2.4\text{V}$ when $I_{OH}=-400\mu\text{A}$. The conservative designer would conclude that the current might be as low as 400 µA and as high as 55 mA; the worst cases. It is possible to go back to the circuit of the gate with 0.8 volts at the output terminal and calculate the current. However, this analysis would be for nominal values only and not provide definitive limits on the current.

Note the notation at the bottom of the specification table in Figure 9. This notation discusses the limit on the amount of time a short circuit is allowed to be connected to the output of some gates. This time limit is based on the amount of time it takes the internal components of the integrated circuit to heat up to its maximum allowed value. While connecting a transistor base to the output is not exactly a short circuit, it is outside the allowed operating region and probably should have the same time limits as the short circuit.

TERMINAL CHARACTERISTICS

During the previous discussions on TTL, we were looking at circuit operation and developing an understanding of how the terminal specifications were arrived at. Let us now take a broader look at these characteristics.

First, the input currents are quite high when the input is low, requiring the driver to sink a lot of current. When the input is high, the input current into the gate is quite low. Thus, any circuit which is supposed to drive the input to a TTL gate must concentrate on sinking current, and only needs to source a little current when the driver output voltage is high.

Second, the output strength of the TTL gate matches the strength requirements at the input. An example is given in Figure 11. The TTL gate can sink a large current when its output is low, but can only source a small current when the output is high. Thus, if the TTL gate is expected to drive a circuit that is not another TTL circuit, you must exercise care when designing the interface. The load circuit must not require large input currents when its input is high, but may use larger currents when the input voltage is low.
When driving other TTL gates as loads, a 7400 gate must be able to sink more current than it needs to source.

These requirements must be kept in mind when designing interfaces with the TTL gate at both the input and the output. Examples of interfacing with TTL gates are shown in Figure 12 and 13. See data books for more complete data.
Figure 12. Several ways to drive loads from TTL gates.

Figure 13. Several interfaces to drive TTL gates.
WIRED-AND CONNECTION

Because the active pull-up or totem-pole output of the TTL gate always has one transistor
cutoff and the other turned on, you cannot connect two outputs together. If one is trying
to pull the output high, and the other is trying to pull it low, you will have a very low
impedance path to ground and very large currents.

For the same reason, the output must not be connected to any voltage source or to ground
through a low impedance path. In one state or the other, there would be a low impedance
path and large currents.

OPEN COLLECTOR GATES

In order to overcome the limitations created by the totem pole output circuit, some gates
are manufactured with the output collector left open. One example is the 7405, a quad 2-
input NAND gate with open collector outputs. If you connect a resistor as the pull-up,
you can use this resistor to source current when the output is high and/or you can wire-
AND the collectors together.

TTL FAMILIES

As the designers of TTL gates became more sophisticated, they developed modifications
which would provide special characteristics. The original series of TTL was designated
as 74XX, where the XX is replaced by logic function ( 00 is a quadruple 2-input NAND,
04 is a hex inverter, etc.) The 74LXX series is a low power family. 74HXX is a high
speed family. 74SXX is a family based on Schottky diodes and transistors. 74LSXX is a
family of low power Schottky. A 54xXX is also provided as a companion family to the
74xXX families. The 54... families are identical to the 74... families, except for operating
temperature range and tolerance on power supply voltage.

Each family has different characteristics, but the same logic functions. The L family is
low power, but is much slower than the standard family. The H family is high speed, but
also has higher power dissipation. The Schottky families are quite fast without increasing
the power dissipation. More recent advances in TTL family have given us several other
versions. For example, 74F, 74AS, and 74ALS, for Fast, Advanced Schottky, and
Advanced Low-power Schottky. The AS family is the fastest, with a propagation delay of
less than 5 ns. Table 2 shows the propagation delays and power supply current for each
type of gate. The power supply current, I_{CC}, is the average for a 50% duty cycle with the
output spending half its time low and half the time at a high.

In addition, these different families use slightly different circuit configurations. A little
study of the circuits will reveal the same operations.
Table 2. Propagation delays and power supply current for TTL families
Data abstracted from Texas Instruments TTL Data Books

<table>
<thead>
<tr>
<th>Gate</th>
<th>t_{PLH} (ns)</th>
<th>t_{PHL} (ns)</th>
<th>I_{CC} (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>min</td>
<td>typ</td>
<td>max</td>
</tr>
<tr>
<td>7400</td>
<td>11</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>74L00</td>
<td>35</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>74H00</td>
<td>5.9</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>74LS00</td>
<td>9</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>74S00</td>
<td>2</td>
<td>3</td>
<td>4.5</td>
</tr>
<tr>
<td>74ALS00</td>
<td>3</td>
<td>11</td>
<td>2</td>
</tr>
<tr>
<td>74AS00</td>
<td>1</td>
<td>5</td>
<td>1</td>
</tr>
</tbody>
</table>

SCHOTTKY TTL

A Schottky PN junction is made up of a semiconductor and a metal. This kind of junction has two characteristics: low turn-on voltage and low junction capacitance.

When a Schottky junction is used in place of or in parallel to the Base-Collector junction of a transistor, the transistor is faster because of the lower junction capacitance and because the transistor cannot go so deep into saturation. Because the turn-on voltage for the BC junction is lower, $V_{CE_{sat}}$ is higher.

Schottky TTL is thus faster than standard TTL and the terminal voltages are slightly different. See the data sheet.

TRI-STATE OUTPUT

The totem-pole output of a TTL gate provides additional speed at lower power for the gate than a simple pull-up resistor. The cost, however, is that the gate outputs cannot be connected in parallel. This problem is serious when you need to make a bus structure such as a data bus, where several gates need to put data onto the bus at different times. The outputs can be OR'd or AND'ed using appropriate gates, but this solution is less than satisfactory and slows down the operation.

A better solution is the TRI-STATE output as shown in Figure 14. The added input allows normal operation of the gate when the "enable" input is high. Both output transistors are cutoff when "enable" is low.