CASCADED COUNTERS

Counter circuits can be cascaded to increase both the modulus of the count sequence and the frequency division. Large counter applications requiring several stages of cascaded counters include digital time clocks, frequency dividers, and synchronization circuits.

The simplest example of cascaded counter stages is an asynchronous counter. The individual toggle flip-flop stages of an asynchronous counter are MOD-2 counters. MOD-2 counters are cascaded by routing the output of one stage into the clock input of the next stage. With each cascaded stage, the modulus of the counter increases. The final modulus of the counter is equal to the modulus of the individual stages multiplied together. Thus, a 4-bit asynchronous counter has a modulus of **2 x 2 x 2 x 2 = 16**. The output frequency from the final stage is equal to the input frequency divided by the modulus. A simplified block diagram of the cascaded counter stages is shown in Figure (29). The input clock frequency is divided by 2 at each stage.

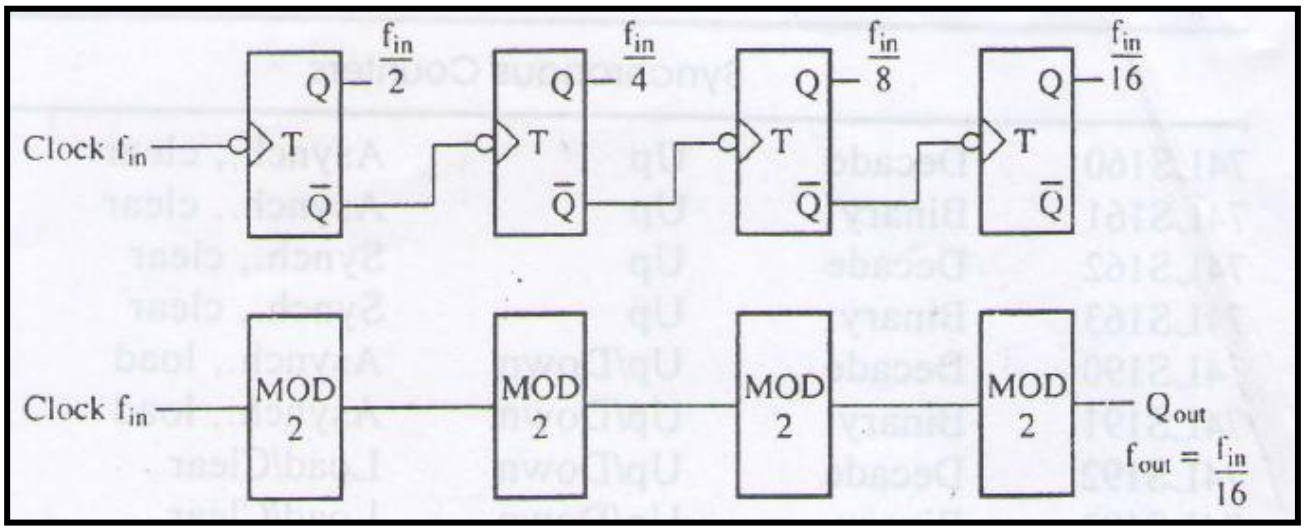

Figure (29): Cascaded MOD-2 Counters.

The 74LS90 IC counter is an example of a counter circuit that requires cascading in order to obtain a decade counter. The decade counter is formed by cascading a MOD-2 counter with a MOD-5 counter. The final modulus is 2x5, or 10.

Several 74LS90 counters could be cascaded together to obtain MOD-10, MOD-100, and MOD-1000 counters. The most significant output bit, Q_D, is used as the cascaded clock input to the next stage; Figure () shows a simplified block diagram of MOD-10 counters cascaded together.

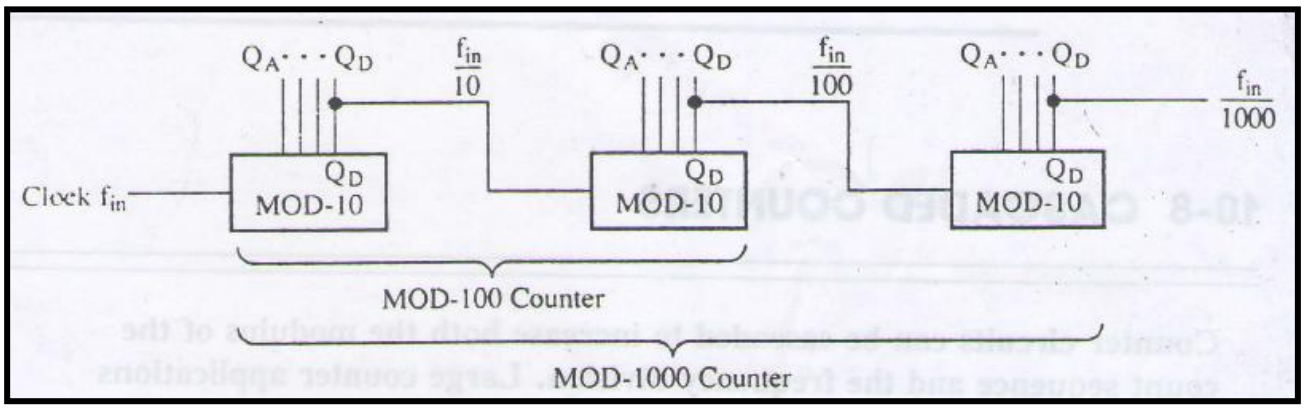

Figure (30): Cascaded MOD-10 Counters.

Synchronous counters can be cascaded by maintaining a common clock signal to all count stages and by routing a ***ripple carry output (RCO)*** from one stage to a count enable input in the next counter stage. Synchronous counters such as the 74LS160, 74LS161, 74LS162, and 74LS163 have ripple carry outputs and ***count enable inputs*** to ensure synchronous operation through all the cascaded count stages. An example of synchronous counter cascading using the ripple carry out and count enable is shown in Figure (31).

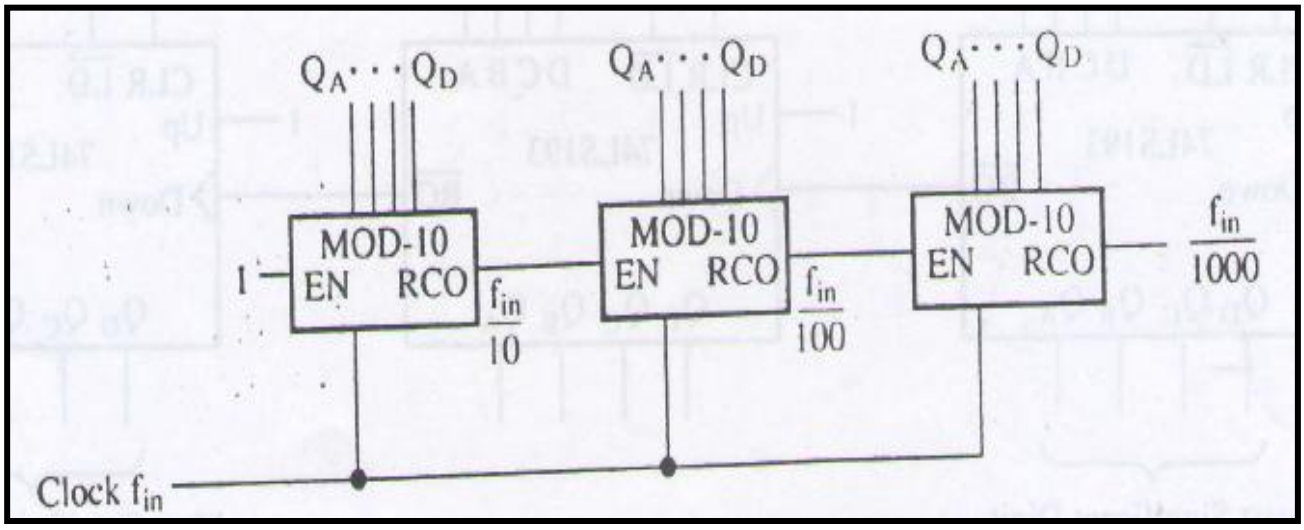

Figure (31): Synchronous Counter Cascading.

The modulus of the cascaded counter is not limited to a multiple of the full modulus of the counters in the cascaded circuit. It can be fine-tuned to be any integer value by presetting or clearing the count stages as required. By presetting the count stages, we find that the final modulus obtained from the cascaded circuit is equal to the maximum modulus minus the initial state.

Counter Modulus:

Desired modulus = maximum modulus - initial state.

EXAMPLE (17): Cascaded Counter

Problem: Design a divide-by-365 counter using 74LS193 counters.

Solution: Three 74LS193 counters are needed for the design. The maximum modulus of three cascaded 74LS193 counters is:

16 x 16 x 16 = 4096.

The desired modulus is 365. To determine the initial state required to preset the counters to obtain a MOD-365 counter, subtract the desired modulus from the maximum modulus:

4096 - 365 = 3731

The 74LS193 counters generate 4-bit binary numbers; each counter-can be considered a hexadecimal counter. The initial setting, $(3731)_{10}$ should be converted to its hexadecimal equivalent.

$$(3731)_{10} = (E93)_H = (1\ 1\ 1\ 0\ \ 1\ 0\ 0\ 1\ \ 0\ 0\ 1\ 1)_2.$$

The initial setting for the most significant counter stage is ***1 1 1 0***. The next stage is preset for ***1 0 0 1***. The least significant counter stage is set to ***0 0 1 1***. The MOD-365 circuit is shown in Figure (32).

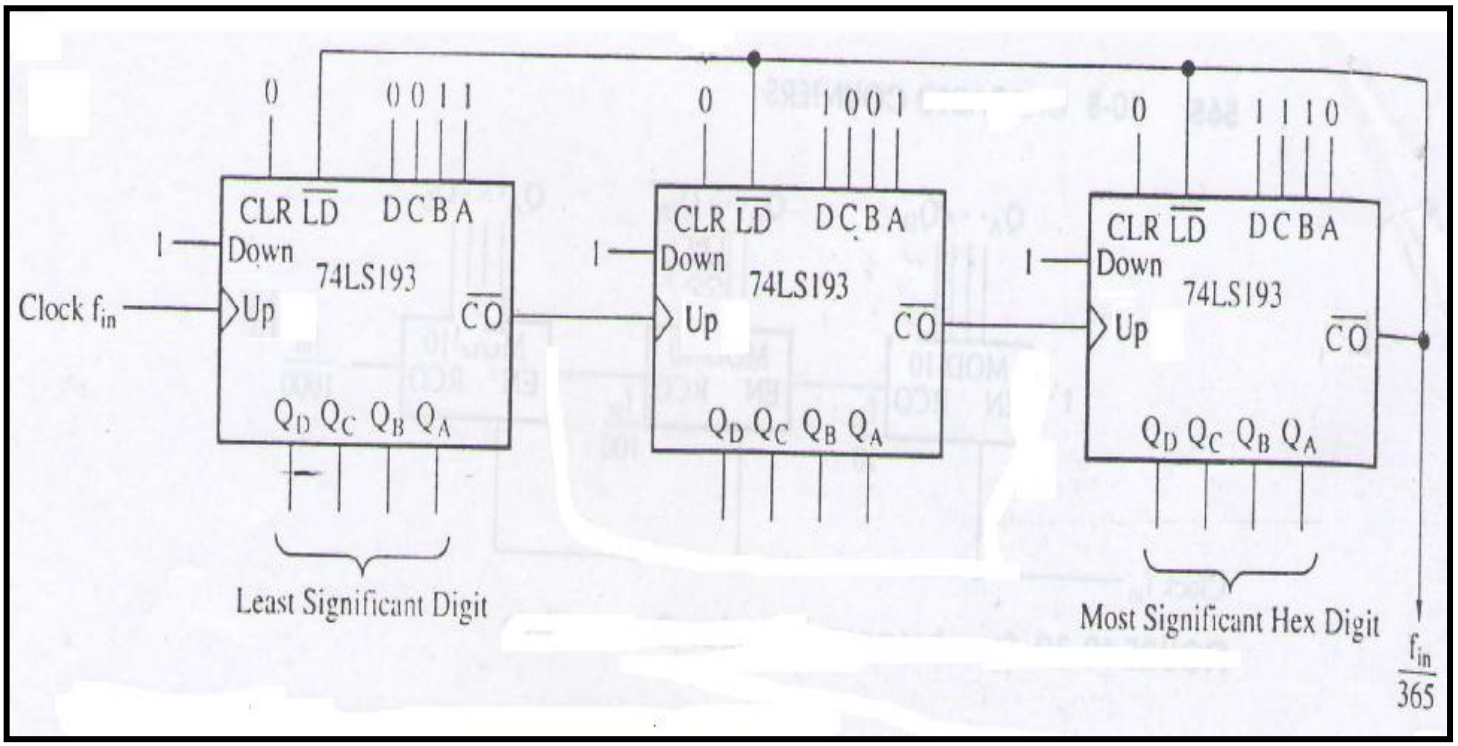

Figure (31): Synchronous Counter Cascading.