THE TRANSISTOR AS AN INVERTER/SWITCH

The utility of a BJT in digital circuits is the ability of the transistor to block or conduct current with just a small control current. Thus, we are primarily interested in the cutoff and saturation modes of operation. In this section, we will discuss the transistor used both as a switch and as a linear inverter.

To start the discussion, we will consider the circuit in Figure 11. This circuit is the classic switch. The operation of the transistor is controlled by the current in the base circuit. Thus, the input voltage controls the circuit. We will analyze the circuit for three cases: V_{in} =0, 5, and 10 Volts.

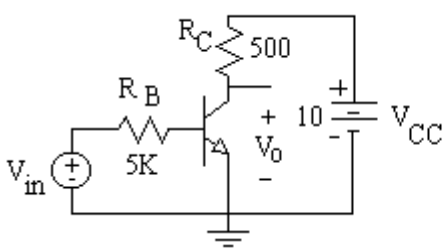
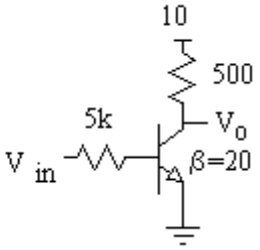


Figure 11. Transistor Switch.



Simplified Drawing.

$V_{in} = 0$

Because the base-emitter junction is a diode, this part of the circuit can be analyzed as we did earlier for diode circuits. With no source voltage to overcome the turn-on voltage of the diode, there will be no current flow. With no base current, the transistor is cutoff and there will be no collector current. See the circuit in Figure 12 where the transistor has been replaced with its cutoff model. With no current in the collector circuit, there will be zero voltage drop across the collector resistor. Hence the voltage between the collector and emitter will be

$$V_{CE} = V_O = V_{CC} = 10 \text{ Volts.} \qquad (1)$$

(Note the order of the subscripts, CE. A positive voltage for V_{CE} means that the collector is more positive than the emitter.)

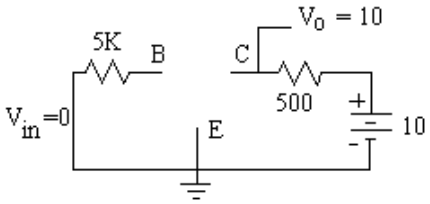


Figure 12. Circuit With V_{in} = 0. The transistor is replaced with its cutoff model.

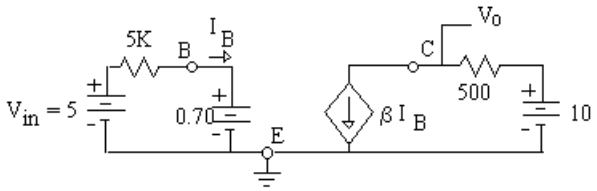


Figure 13. Circuit With V_{in} = 5 Volts

V_{in} = 5 Volts

An analysis of the base circuit in this case indicates that the base current is not zero. From Figure 13,

$$I_B = \frac{V_{in} - V_{BE}}{R_B} = \frac{5 - 0.7}{5K} = 0.86 \text{ mA} \qquad (2)$$

Since there is base current, there must be collector current. If we assume the transistor is in the active region, the active circuit model has replaced the transistor in Figure 13. We can solve this circuit for the collector current.

$$I_C = \beta I_B = 20 * 0.86 = 17.2 \text{ mA} \qquad (3)$$

The final information we would like to know is the output voltage, the voltage at the collector . We cannot get V_{CE} directly, we have to use the voltage drop across the collector resistor;

$$V_O = V_{CE} = V_{CC} - I_C R_C = 10 - 17.2 \text{ mA} * 0.500 \text{ K}\Omega = 1.4 \text{ V} \quad (4)$$

Since $V_{CE} > V_{CEsat}$ (=0.2V), this result is consistent with the assumption that the transistor is operating in the active region.

Now let us look at the final case.

V_{in} = 10 Volts

If we assume the transistor will be in the active region, the process will be the same as for the previous case. We can look at Figure 13 but with the input voltage at 10 volts.

$$I_B = \frac{V_{in} - V_{BE}}{R_B} = \frac{10 - 0.7}{5K} = 1.86 \text{ mA} \qquad (5)$$

Proceeding to the collector circuit, we will attempt to find the collector current as we did before;

$$I_C = \beta I_B = 20 * 1.86 = 37.2 \text{ mA} \qquad (6)$$

The output voltage is then,

$$V_O = V_{CC} - I\,R = 10 - 37.2 * .500 = -8.6 \text{ Volts ??} \quad (7)$$

This result says that the output voltage is negative. How can that possibly be? There is no source for the negative voltage; no negative power supply. The transistor is modeled as a current-controlled current source, but is not a current generator. It can only work within the limits of the power supplies. You will note on the collector characteristic curves that the collector voltage cannot go negative with a positive collector current. The obvious conclusion is that the transistor circuit has saturated, and the active region model is no longer valid.

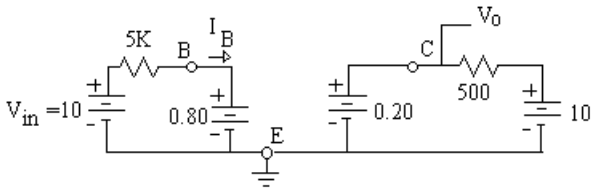


Figure 14. Circuit in Saturation

If we go to the saturation region model, the circuit is shown in Figure 14. Note that the only base circuit change is to change V_{BE} to 0.80 volts. This change makes the base current

$$I_B = \frac{10 - 0.80}{5K} = 1.84 \text{ mA} \quad (8)$$

We can also determine the collector current,

$$I_C = \frac{V_{CC} - V_{CEsat}}{R_C} = \frac{10 - 0.20}{0.5K} = 19.6 \text{ mA} \quad (9)$$

We already know that the output voltage is 0.2 Volts ($=V_{CEsat}$) since the transistor is in saturation. The only thing left is to verify that the model used is appropriate for the situation. (We already know the active region model is inappropriate, and that we are not in cutoff, $I_B > 0$.) To demonstrate that the saturation model is appropriate, we need only show the $I_{Csat} < \beta I_B$. Since $\beta I_B = 36.8$ mA > 19.6, the saturation model is appropriate.

SUMMARY

It is appropriate at this time to explicitly define the criteria for operation in each mode.

Cutoff: $V_{BE} < V_{BE\gamma}$ and $V_{BC} < V_{BC\gamma}$

If this condition occurs, the base current will be zero and the collector current will be zero. Of course, we are ignoring the leakage currents. We are also not considering the possibility of using the transistor backwards with collector and emitter reversed. Thus, we are assuming that the collector voltage is more positive than the base voltage. We will discuss the value of $V_{BE\gamma}$ later.

Active Region $I_B > 0$, $V_{BE} = 0.70$, $I_C = \beta I_B$, $V_{CE} > 0.2$ V.

Saturation Region: $I_B > 0$, $V_{BE} = 0.80$, $V_{CE} = 0.2$, $I_C < \beta I_B$.

The value of $V_{BE\gamma}$ we choose will have a significant bearing on how we view the transition between cutoff and the active region. For logic systems, we will use $V_{BE\gamma}$ = 0.50 Volts. This is the value the base-emitter voltage must be less than to guarantee the transistor is cutoff. Note that when the transistor is saturated, V_{BE} =0.80. For logic systems, any value in between is indeterminate. This inconsistency will not cause us any trouble in logic systems. However, this discrepancy will cause some difficulty when we are trying to find the transition between cutoff and active operation and between active and saturation operation.

APPENDIX A

DEFINITION OF TERMS FOR LOGIC GATE SPECIFICATIONS

V_{inLmax} The maximum input voltage that will be seen as a "LOW".

V_{inHmin} The minimum input voltage that will be seen as a "HIGH".

V_{oL} Output voltage when the output is "LOW". Spec's often give a V_{oLmax} which is the maximum value you will normally find, considering component variations.

V_{oH} Output voltage when the output is "HIGH".

Note that the output voltage specifications are given under some specific current condition, usually maximum current. The V_{oH} term is almost always associated with I_{oH}.

I_{inL} The current entering the input terminal when the input voltage is low. Normally specified at a fixed input voltage (Usually at V_{oL}). This current is usually negative; leaving the input terminal.

I_{inH} The current entering the input terminal when the input voltage is high. In the cases of DTL and TTL circuits, the input current is specified at maximum input voltage which results in maximum input circuit.

I_{oH} The current entering the output terminal when the output voltage is high. Note that this current is usually negative, the current actually leaves the output terminal. This current is usually specified when the output voltage is at its minimum, high-level value, V_{oHmin}. What this definition means is that this is the maximum current you can take out of the output and still have the output voltage stay at or above the minimum specified value.

I_{oL} The current that the gate can sink when the output is low. Since the gate usually has a transistor driver at the output, the low-level output occurs when the transistor is saturated. Thus, this current is specified at the largest current that the transistor can sink and still stay in saturation. As discussed in the book, while the transistor is in saturation, the voltage rises as the current increases. Thus, this current is usually specified at some specific V_{oLmax}, the maximum output voltage when the output is low (and sinking this large current).

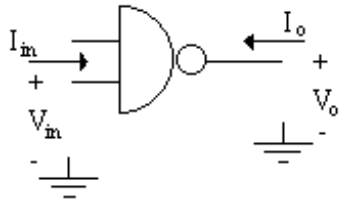


Figure A1. Terminal definitions

Current polarity is defined as positive going into a terminal. Voltages are measured from the terminal to ground. The subscript refer the terminal and its logic level. For example, I_{oL} is the output current when the output is low. and I_{inL} is the input current when the input is low.

APPENDIX B

NOISE MARGINS

NML Noise Margin Low. NML = V_{inLmax} - V_{oLmax}. This is the amount of noise voltage that can appear on the low level output signal of a gate and still have that low level signal be guaranteed to be recognized as a low at the input of a load gate.

NMH Noise Margin High. NMH = V_{oHmin} - V_{inHmin}. This is the amount of noise voltage that can appear on a high level signal at the output of a gate and still have that high level signal be guaranteed to be recognized as a high at the input of a load gate.

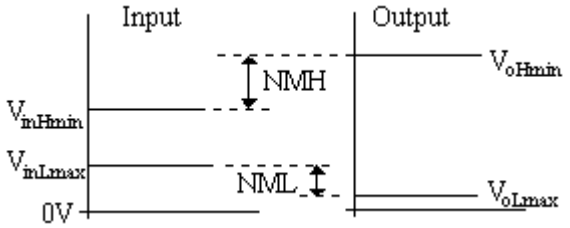


Figure B1. Definition of noise margins

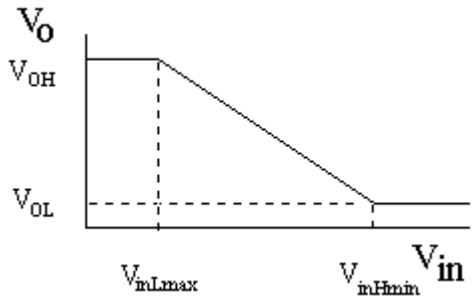


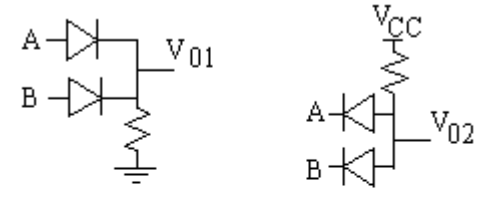
Figure B2. Typical voltage transfer characteristic for an inverting gate

DIODE TRANSISTOR LOGIC

Resistor-Transistor Logic was an early form of logic used in the 1950's and early 1960's. RTL was made from discrete transistors and resistors and manufactured on printed circuit boards with several gates per board. These boards were plugged into board sockets with wiring on the socket pins determining the system function. RTL was a big improvement over vacuum tube technology previously used, requiring less than one quarter the space and one tenth the power dissipation. RTL was superceded in the 1960's by Diode-Transistor Logic and then Transistor-Transistor Logic, DTL and TTL respectively. DTL was initially made with discrete transistors and resistors before being integrated onto silicon. One early form of DTL, used by IBM Corp in the 360 family of computers, was really a hybrid technology. Transistor and diode chips were glued to a ceramic substrate and aluminum resistor paste was deposited on the substrate to make resistors. Finally the ceramic base and components were hermetically sealed in an aluminum can. This family was used extensively in IBM products in the middle to late 1960's. While this family was not a true integrated circuit, it was very successful and was less expensive than true integrated circuits for several years. By the early 1970's integrated circuits became quite common and DTL gave way to TTL which was more appropriate to integrated circuit technology.

While DTL is no longer commercially used, we will discuss it because it is similar to and easier to understand than TTL, and because designers still find the configuration of value. First, however, we will discuss diode logic which is the front end of the DTL gate and performs the actual logic operation.

DIODE LOGIC



A	B	V_{01} = A+B
L	L	L
L	H	H
H	L	H
H	H	H

A	B	V_{02} = A•B
L	L	L
L	H	L
H	L	L
H	H	H

Figure 1. Diode logic and truth tables

Two diode logic configurations are shown in Figure 1. The truth tables show that the first circuit performes a logical OR and the second circuit performs a logical AND. One problem with these circuits is that there is a voltage level shift through the circuit. If several circuits are cascaded as shown in Figure 2, the output voltage for each stage is approximately one diode voltage drop further away from the rail. Logic "0" rises for the

AND gate and logic "1" drops for the OR gate. Only a limited number of series cascaded circuits can be used before the logic levels must be restored to the rails. Even more serious is the voltage degradation for the cascaded AND-OR function.

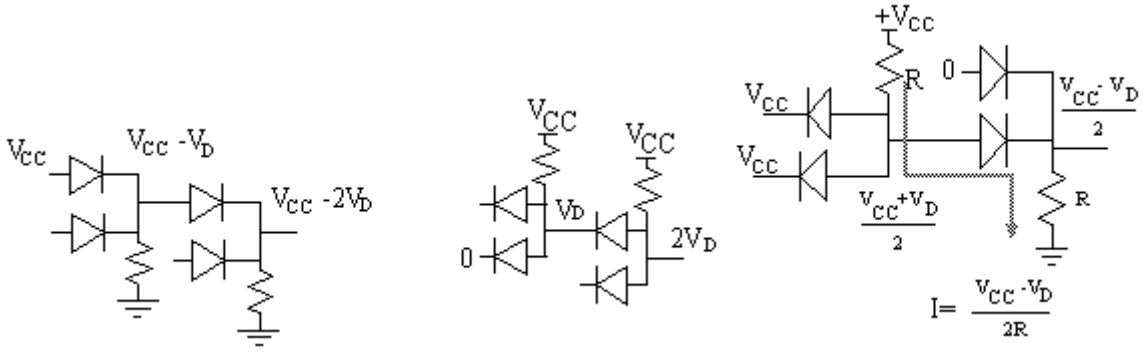


Figure 2. Cascaded diode logic showing level shifts.

The obvious way to restore the logic level voltages is to use a double transistor inverter. However, it does not take a genius to notice the a single inversion on the end of each gate will make a NAND or a NOR gate and the logic level is automatically restored for each gate. The NAND gate is used extensively. As you no doubt recall, any logic expression can be implemented using just NAND gates. Thus, other forms are not necessary.

DIODE TRANSISTOR LOGIC CIRCUITS

A typical DTL NAND gate is shown in Figure 3. Observe the diode AND function on the front end and the transistor NOT at the output end. The extra resistors and diodes are used to maintain appropriate currents, to maintain proper functioning, and to guarantee certain noise margins. We will completely analyze this circuit, but will be particularly interested in the "terminal" characteristics of the gate. Our ultimate goal is to understand the operation of the gate so that the manufacturer's specifications can be understood.

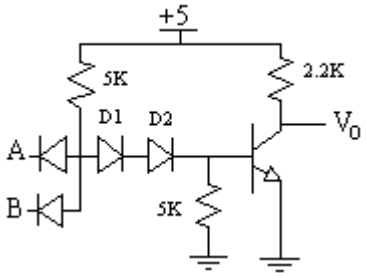


Figure 3. DTL Circuit

ANALYSIS OF THE DTL GATE

Analysis of the DTL gate is dependent on complete understanding of the currents within the gate under all logic conditions. First let us develop a generic understanding of the operation. *Of particular importance will be the direction of currents at the terminals of the gate*. As in most logic systems, the transistor will either be cutoff or saturated.

If all inputs are high, (+5v), no current will come out of the input diodes at the input and current will flow down through the first 5K resistor and through the diodes D1and D2 toward the base of the transistor. Some current will split off and go down through the lower 5K resistor to ground. However, most of the current will go into the base of the transistor causing it to saturate, pulling the output low, V_O =0.2 Volts. We will show this condition quantitatively shortly.

If one or more of the inputs to the gate are held low (0.2 V), then the current down through the 5K resistor will go out the input diode, away from the transistor base. Under this condition, the transistor will be cutoff and the ouput will be high with V_O =5 Volts.

ANALYSIS WITH INPUT LOW

Quantitatively, we will start with one or more inputs held low, at 0.2 Volts. From the logic function of the NAND gate, we know that the output is supposed to be high. Therefore, the transistor must be cutoff. To begin with, we will assume the two diodes D1 and D2 in series will also be cutoff. All the current coming down through the 5K resistor must all go out through the input diode, causing it to be on. The circuit with the models indicated is shown in Figure 4. From this circuit we can calculate all voltages and currents and prove (or disprove) our assumptions about the condition of each element.

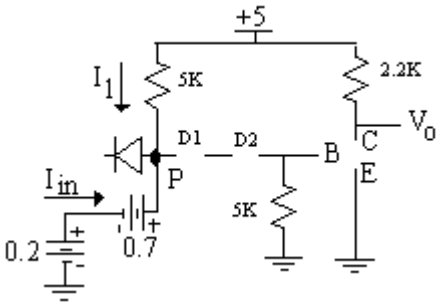


Figure 4. DTL gate model with input low

The voltage at point P is

$$V_P = 0.2 + 0.70 = 0.90 \text{ Volts.}$$

We need to show that this voltage is low enough that the two series diodes and the transistor will be cutoff. The argument is that if either diode carries current, then both must. Since 0.9 Volts is not enough across the pair to maintain conduction, then neither conducts. Given that the diodes are off, then the voltage at the base of the transistor is zero, and is also cutoff. We can verify that the input diode is conducting by observing that current I_1 is

$$I_1 = (5\text{-}0.9)/5K = 0.82 \text{ mA}$$

This current leaves through the input diode, hence it is on. The current entering the input terminal is

$$I_{in} = -I_1 = -0.82 \text{ mA}$$

The negative sign occurs because the input current is defined as going into the terminal.

We can now verify that the output voltage is 5 Volts because the transistor has been shown to be cutoff. Thus,

$$V_O = 5.0 \text{ Volts}$$

One other characteristic of the DTL gate that can be obtained at this point is the range of input voltages that will be recognized as a "low". From the logic function of the NAND gate, this can be translated into the question of how high the input voltage may rise and still keep the transistor cutoff.

The transistor will remain cutoff as long as the voltage at the base does not rise above 0.5 volts. At this voltage, there will be current down through the lower 5K resistor to ground. This current must come from the +5 supply down through the upper 5K resistor and the diodes, D1 and D2. Hence the diodes must be conducting. This current will be 0.1 mA. The voltage at point P will be

$$V_P = 0.5 + 0.7 + 0.7 = 1.9 \text{ Volts}$$

The current I_1 is

$$I_1 = (5-1.9)/5K = 0.62 \text{ mA}$$

The current going out through the input diode will be

$$I_{in} = -(0.62 - 0.1) = -0.52 \text{ mA}$$

indicating that the input diode is still conducting. Figure 5 shows the resulting circuit with the circuit models included. The maximum voltage at the input that is guaranteed to be recognized as a low is

$$V_{inLmax} = 1.9 - 0.7 = 1.2 \text{ Volts.}$$

This result is included in the table of terminal specification at the end of this chapter.

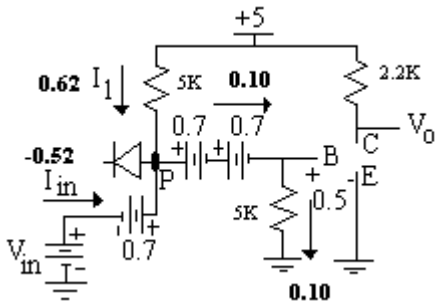


Figure 5. DTL circuit model with $V_{in} = V_{inLmax}$

ANALYSIS WITH ALL INPUTS HIGH

When all inputs are high, all current down through the upper 5K resistor will go toward the base of the transistor, causing it to saturate. The series diodes will obviously be conducting, and we will show that the input diodes are cutoff. Figure 6 shows the circuit with these models.

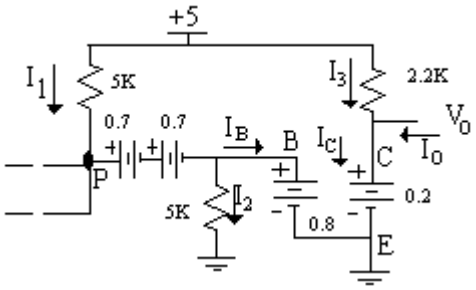


Figure 6. DTL circuit model with inputs high

The voltage at point P is

$$V_P = 0.8 + 0.7 + 0.7 = 2.2 \text{ volts}$$

Thus, I_1 is

$$I_1 = (5\text{-}2.2)/5K = 0.56 \text{ mA}$$

This current will go through the diodes toward the base of the transistor. Some of the current will go down through the lower 5K resistor with the rest going into the base of the transistor. With the transistor saturated, the current going down through the 5K resistor will be

$$I_2 = 0.8/5K = 0.16 \text{ mA}$$

The base current then is

$$I_B = 0.56 - 0.16 = 0.4 \text{ mA}$$

If the transistor is to be saturated, the maximum collector current is

$$I_{Cmax} = \beta I_B = 30 * 0.4 \text{ mA} = 12.00 \text{ mA}$$

at saturation, the current coming down through the 2.2K collector resistor is

$$I_3 = (5\text{-}0.2)/2.2K = 2.182 \text{ mA}$$

this current is much less than the maximum saturation current and we see that with no load, the transistor will, indeed, be in saturation. In fact, there is excess capacity in collector saturation current. This excess capacity can be used to **sink** external load current. This current is called I_o or load current. The maximum load current this gate can sink is

$$I_{oLmax} = 12.00 \text{ mA} - 2.182 \text{ mA} = 9.818 \text{ mA}$$

Note that this current is entering the terminal of the gate, hence, is positive.

CALCULATION OF V_{inHmin} and I_{inH}

We need to go back now and look at the input voltage in Figure 6 and determine the minimum allowable input voltage that will still be recognized as a high, V_{inHmin}. There are several ways we could define this value, but we will use a straightforward definition. That is, we will define the input to be high as long as no current flows through the input diodes. In other words, as long as the input diodes are cutoff. Thus,

$$V_{inHmin} = V_P - 0.60 = 2.20 - 0.60 = 1.6 \text{ Volts.}$$

Since the input diodes must remain cutoff, $I_{inH} = 0$.

CALCULATION OF FANOUT

If several load gates are connected to the output terminal of the gate we are looking at, we need to look at the current output drive capability compared to the input current requirements of the load gates. Because the input current is zero when high, an infinite number of load gates can be driven when high. However, the DTL gate requires current when the input is low. This situation is shown in Figure 7. We made that calculation earlier and found $I_{inLmax} = - 0.82$ mA. Note that this current is negative meaning that it is coming out of the input terminal. We also found the output of a gate can sink 9.818 mA when it is low. We can now calculate the fanout.

$$\text{Fanout} \leq \frac{I_{oLmax}}{I_{inL}} = \frac{9.818}{0.82} = 11.97$$

The maximum number of gates that can be driven as loads is 11.

Fanout = 11

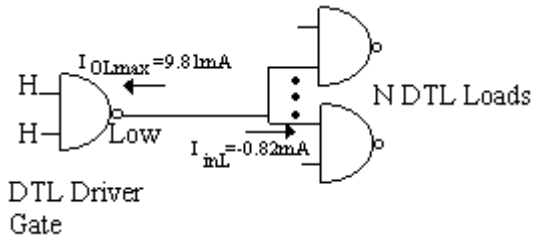


Figure 7. DTL driver gate with N identical DTL load gates

We also need to check voltage compatibility. That is, $V_{oH}>V_{inHmin}$ and $V_{oL}<V_{inLmax}$ which is true as shown in Figure 8 where V_{oH} is given at no load condition because I_{inH} = 0.

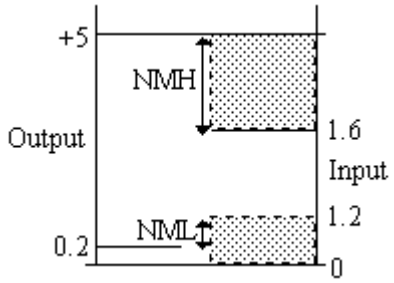


Figure 8. Comparison of output and input voltages for DTL gate.

CALCULATION OF V_{oH} AND I_{oH}

We now have calculated all terminal characteristics except for the output voltage and current when the output is high. Because I_{inH} = 0, with any number of loads there will be zero load curent. Thus, V_{oH} = 5.0 Volts. This specification is satisfactory if the only load is other gates. In many cases, however, we wish to use other types of loads and additional information is necessary.

When the output is high, the transistor is cutoff and any current coming out of the gate will come from the supply through the collector resistor. One way to define the output is when the output is allowed to drop as low as V_{inHmin} (although this is by no means the only way). Using this definition, we can calculate the output current as

$$I_{oH} = -(5-1.6)/2.2K = -1.545 \text{ mA}$$

Again, the negative sign indicates that current flows out.

We now have a complete set of specifications for the DTL gate as shown in Table 1.

Table 1. Terminal Specification for the DTL GATE

V_{inLmax} = 1.2 V	V_{oL} = 0.2
V_{inHmin} = 1.6 V	V_{oH} = 5 (at I_{oH} =0)
	= 1.6 (at I_{oH} = max)
I_{inL} = - 0.82 mA	I_{oLmax} = 9.818 mA
I_{inH} = 0	I_{oHmax} = -1.545 mA (at V_{oH} =V_{inHmin})

Fanout = 11

//
Exercise:
In the above discussion, V_{oH} was allowed to drop all the way to V_{inHmin}. Allowing it to drop this low, makes the high noise margin, NMH = 0. A more appropriate noise margin would be to make NMH equal to the NML. Calculate the I_{oH} under this condition.

(ans. -1.09 mA)

\\\

OTHER LOGIC FUNCTIONS

While the NAND function can be used to implement any logic expression, it is often convenient to use other functions. Figure 9, 10, 11, and 12 show how four other function could be implemented. Figure 9 is the AND function, Figure 10 is the NOR fuction, Figure 11 is the OR function, and Figure 12 is the AND-OR-INVERT, AOI, a very useful function when implementing sum-of-products logic expressions.

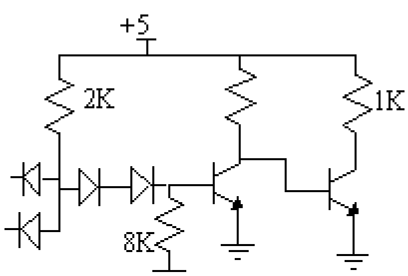


Figure 9. DTL AND gate

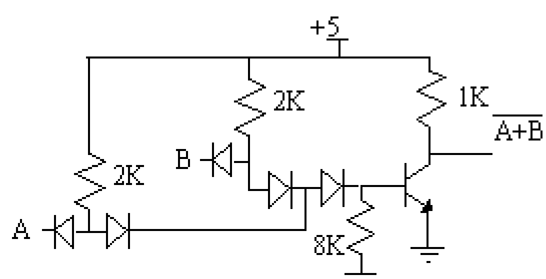


Figure 10. DTL NOR gate

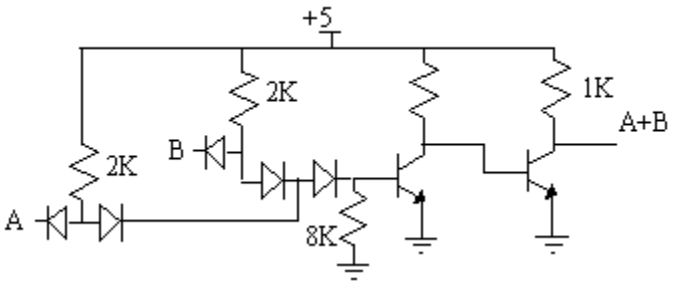


Figure 11. DTL OR gate

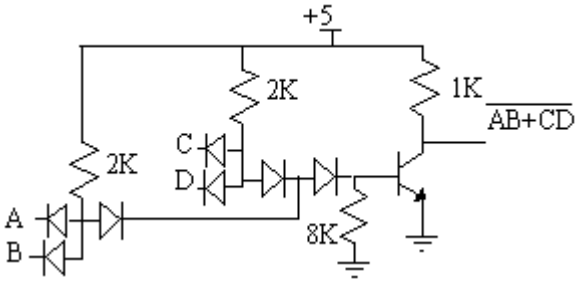


Figure 12 DTL AND-OR-INVERT gate

TRANSISTOR-TRANSISTOR LOGIC

The evolution from DTL to TTL can be seen by observing the placement of p-n junctions. For example, the diode D2 from Figure 2 in the chapter on DTL can be replaced by a transistor whose collector is pulled up to the power supply; transistor Q_2 in Figure 1 below. The p-n junction of D2 is replaced by the BE junction of Q2 and with the current gain of the transistor, the current going into the base of Q3 is greatly increased, increasing the fanout.

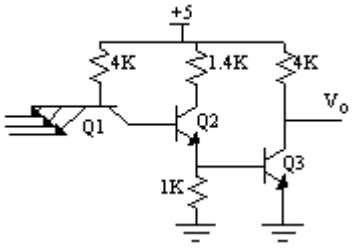


Figure 1. TTL Gate.

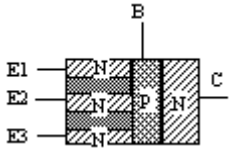


Figure 2. Configuration of Q_1 as a 3-emitter transistor.

The input diodes and D1 are replaced by the multi-emitter NPN transistor, Q1, in Fig. 1 and represented by the drawing in Figure 2. Later on, we will make additional modifications to this curcuit to improve its performance further.

The analysis of this circuit follows very much the same path as the analysis of the DTL gate. For the most part, we will consider the input transistor, Q1, to act just like two diodes. The transistor Q2, however, will operate in all three regions. The treatment of the output voltages and currents will be treated the same as the DTL gate and Q3 will either be cutoff or saturated, corresponding to an output high and an output low, respectively.

ANALYSIS WITH ONE OR MORE INPUTS LOW

With an input low, Q3 should be cutoff. We will assume Q2 is cutoff and then check our assumption. If Q2 is cutoff, then there can be no current coming out of the collector of Q1, hence its base-collector junction can be modeled as an open circuit. The base-emitter junction of Q1 will be conducting. The circuit with these models substituted for the transistors is shown in Figure 3. Note the similarity to the DTL circuit under the same conditions. The two unused inputs are assumed to be high, and are thus, modeled as open. From this case, we can see that V_{oH} = 5 volts with no load, and

$$I_{inL} = -I_1 = -(5-0.9)/4K = -1.025 \text{ mA}$$

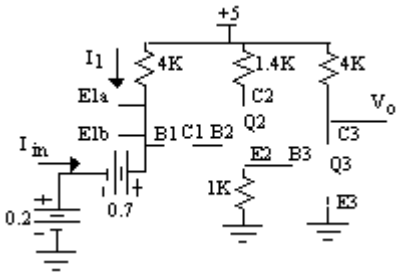


Figure 3. TTL circuit model with one input low.

We turn now to finding V_{InLmax}. We will use the criterion that V_{in} will be considered as a low as long as Q3 is kept cutoff. If the base voltage for Q3 can be raised to 0.5 Volts without turning it on, then there will be 0.5 mA current in the 1KΩ resistor. This current can only come from Q2, which means it must be conducting. Even assuming all this 0.5 mA comes through the collector of Q2, the voltage drop across the 1.4 KΩ resistor will be 0.7 Volts, not enough to cause the transistor to saturate. Thus, the active model for Q2 is appropriate as shown in Figure 4.

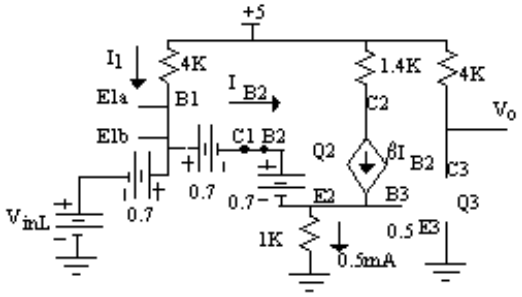


Figure 4. TTL circuit model to determine V_{inLmax}.

If we assume that β=30, the base current in Q2 is

$$I_{B2} = \frac{0.5mA}{\beta+1} = \frac{0.5}{31} = 0.016mA$$

Because this current is coming out of the collector of Q1, the base- collector junction of Q1 is on, and is modeled as a diode in Figure 4.

The voltage at B1, the base of Q1, is

$$V_{B1} = 0.5 + 0.7 + 0.7 = 1.9 \text{ Volts}$$

The current coming down through the 4 KΩ resistor, I_1, is

$$I_1 = \frac{5.0 - 1.9}{4K} = 0.775mA$$

This is considerably more than is going into the base of Q2, therefore, the input BE junction of Q1 will also still be conducting. The maximum voltage at the input is

$$V_{inLmax} = 1.9 - 0.7 = 1.2 \text{ Volts}$$

CALCULATIONS WITH INPUT HIGH

The circuit model for the TTL gate with all inputs high is shown in Figure 5. Both Q2 and Q3 are modeled as saturated, an assumption that must be verified. With the inputs high, Q1 is modeled as two diodes with the B-E diodes cutoff, and B-C diode conducting.

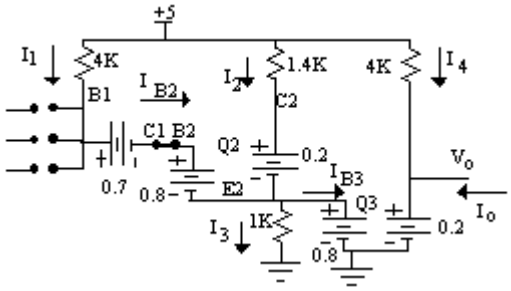


Figure 5. TTL gate circuit model with all inputs high.

The voltage at the base of Q1 is

$V_{B1} = 0.8 + 0.8 + 0.7 = 2.3$ Volts.

The current down through the 4 KΩ resistor, I_1 is

$$I_1 = \frac{5.0 - 2.3}{4K} = 0.675mA$$

All this current goes into the base of Q2.

$I_{B2} = 0.675$ mA

If Q2 is saturated, voltage at its collector terminal is

$V_{C2} = 0.8 + 0.2 = 1.0$ Volts

And the collector current is

$$I_{C2} = I_2 = \frac{5.0 - 1.0}{1.4K} = 2.857mA$$

Clearly, if $\beta = 30$, $\beta I_{B2} > I_{C2}$, and, therefore, Q2 is saturated.

The current coming out of the emitter of Q2 is the sum of the base and collector currents. Part of this current will go down through the 1 KΩ resistor to ground and the rest will enter the base of Q3.

$I_{B3} = I_{B2} + I_{C2} - I_3 = 0.675 + 2.857 - 0.8 = 2.732$ mA

The maximum collector current that Q_3 can carry and still be in saturation is βI_{B3} =81.96 mA, assuming β=30. The maximum current the gate can sink when the output is low

$$I_{oLmax} = I_{Csatmax} - I_4 = 81.96 - 1.2 = 80.76 \text{ mA}$$

Now let's turn our attention back to the input and determine V_{inHmin} and I_{inH} . We will define the input voltage to be high as long as no current goes out the input terminal. Thus, all we have to do is keep the input voltage high enough so that the B-E p-n junction of Q1 does not turn on. Thus,

$$V_{inHmin} = 2.3 - 0.6 = 1.7 \text{ Volts}$$

CALCULATION OF I_{inH}

With the input voltage at a high, say 5 volts, the transistor Q1 will be operating in the reverse active mode. The B-E junction is reverse biased, and the B-C junction is forward biased with a base current of 0.675 mA. If there were significant curent gain, you would expect to see a large current going into the input. However, the reverse β is typically on the order of 0.02. Thus,

$$I_{inH} = \beta_R * I = 0.02 * 0.675 = 0.0135 \text{ mA}$$

This current would add to the current going into the base of Q2, but is ignored because it is quite small and because β_R is made as small as possible and this input current is a maximum and cannot be counted on.

THE TOTEM POLE OUTPUT STAGE

One of the problems with the TTL gate circuit we have been analyzing is that the pull-up resistor on the output transistor will prevent rapid charging of any wiring capacitance on the output. One way to improve the rise time is to reduce the resistance value as is often done, but this also increases the power dissipation when the output is low.

If we look at the circuit, we observe that when the transistor is saturated, it presents a very low effective resistance to ground. The problem arises when the output is high and the pull-up resistor is too large. Ideally we would like to have a very low resistance pull-up when the output is high, but a very high pull-up resistance when the output is low. In this way, we could get quick charging and very low power dissipation. The totem-pole output stage for TTL, shown in Figure 6, does just that.

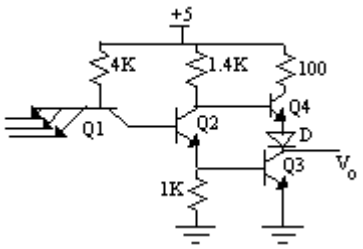


Figure 6. TTL gate with totem-pole output.

This circuit operates just like the original circuit except that Q_4 is on when the output is high and off when the output is low. We need to verify this operation.

OUTPUT LOW

Figure 7 shows the TTL circuit with all inputs high and the output low. The models for the transistors are shown as before, except diode D and transistor Q_4 are added and shown as cutoff.

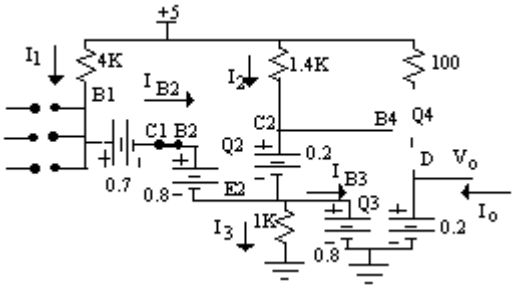


Figure 7. TTL gate with totem-pole output circuit model with inputs high.

The analysis of this circuit proceeds exactly the same as before. The currents, I_1, I_2, I_3, and I_{B3} are the same as before. With the diode and Q_4 not conducting, I_{oLmax} is now the same as I_{C4max} , 81.96 mA. We only need to show that the diode D and transistor Q_4 are indeed off.

The voltage at the bottom of the diode is 0.2 Volts and the voltage at the base of Q_4 equal to the voltage at the collector of Q_2; V_{C2} = (0.2 + 0.8) = 1.0 Volts. Thus, the voltage across the B-E junction of Q_4 plus the diode is 0.8 Volts. If one conducts, the other must also. To take both out of cutoff would require at least 0.5 + 0.6 = 1.1 Volts. Thus, both are off.

OUTPUT HIGH

This condition occurs when one or more inputs are low. The circuit is shown in Figure 8 with the appropriate models used for the transistors and the diode. In this case, Q2 and Q3 are both cutoff while Q4 and the diode are conducting. We have to assume here that there is some load and that the output current is not zero.

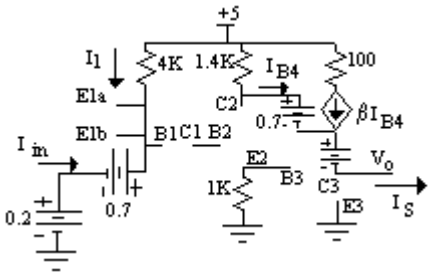


Figure 8. TTL totem-pole circuit model with output high.

The current coming out the output terminal I_S (=-I_o) is the sum of the currents coming down through the base and the collector. Thus,

$I_S = I_{B4} + \beta I_{B4}$

Because each TTL load represents 13 μA, if we assume there are 10 loads, then I_S = 130 μA. The base current is

$$I_{B4} = \frac{130\mu A}{1+\beta} = 4.2\mu A$$

where we have assumed a β of 30. Then taking the path down through the 1.4 KΩ resistor to the output. the output voltage is

$V_o = 5.0 - 4.2\mu A * 1.4K - 0.7 - 0.7 = 3.6$ Volts

The voltage drop across the 1.4 KΩ resistor is neglegible. Of course as the current increases, the output voltage will drop further.

TERMINAL SPECIFICATIONS OF THE TTL GATE

We are now ready to make the table showing the terminal specifications for the TTL gate. These are shown in Table 1.

Table 1. Terminal Specifications For TTL

V_{inLmax} = 1.2 V	V_{oL} = 0.2
V_{inHmin} = 1.7	V_{oH} = 3.4 (@I_o = -130 μA)
I_{inL} = -1.025 mA	I_{oLmax} = 81.96 mA
I_{inH} = 13 μA	I_{oH} = undetermined

TTL DATA

Recommended Operating Conditions

	74	74H	74L	74LS	74S	Units
$V_{CC(rec)}$ — $V_{CC(max)}$	4.75-5.25	4.75-5.25	4.75-5.25	4.75-5.25	4.75-5.25	V
I_{OH}	-400	-500	-200	-400	-1000	μA
I_{OL}	16	20	3.6	8	20	mA
Operating Free-Air Temperature Range	0 - 70	0 - 70	0 - 70	0 - 70	0 - 70	°C

Electrical Characteristics Over Recommended Operating Temperature Range

	Condition	74	74H	74L	74LS	74S	Units
$V_{IH(min)}$		2.00	2.00	2.00	2.00	2.00	V
$V_{IL(max)}$		0.80	0.80	0.70	0.80	0.80	V
$V_{OH(min)}$	@ I_{OH} = max	2.40	2.40	2.40	2.70	2.70	V
$V_{OL(max)}$	@ I_{OL} = max	0.40	0.40	0.40	0.5	0.5	V
$I_{IH(max)}$		40	50	10	20	50	μA
$I_{IL(max)}$		-1.60	-2.00	-0.18	-0.40	-2.00	mA
I_{OS}	*	-20 - -55	-40 - -100	-3 - -15	-20 - -100	-40 - -100	mA

* Not more than one output should be shorted at a time and for H, LS, and S series, duration of short should not exceed one second.

Figure 9. Data for ‘00, ‘04, ‘10, and ‘30 NAND gates for several TTL families (Abstracted from Texas Instruments TTL Data Book.)

MANUFACTURER'S DATA SHEETS

The terminal specifications of several TTL families are shown in Figure 9. You will note the values given for various voltages and currents are quite different from those we calculated. This difference comes from the fact that manufacturing tolerances and variations cannot be closely controlled, hence, the specifications given by the manufacturers are much more conservative than our calculations which were based on nominal values. Also note that the limits are usually given as a maximum or a minimum, depending on which limit is normally used in design. For example, I_{inLmax} is given as -1.6 mA for the 74xx series. What this means is that as a designer, your driver must be able to sink as much as 1.6 mA when the input to the gate is pulled low.

You will note that the TTL gate is rather loosely specified. The question invariably arises as to how one reads the data sheets or designs with this data. Figure 10 shows the allowed operating regions for a 7400, 2-input NAND gate. The best description of these operating regions is probably given by the following examples.

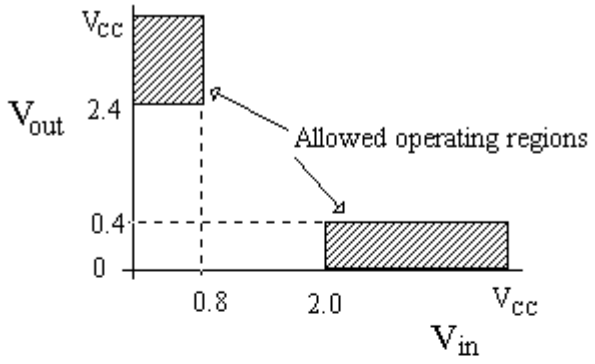
Example 1: If the input voltage is between 0.00 and 0.08 volts, the output voltage will be below V_{CC} and above 2.4 volts as shown in Figure 10a.

Example 2: If the input voltage is between 2.00 and V_{CC}, the input current will be between 0 and 40 μA as shown in Figure 10b.

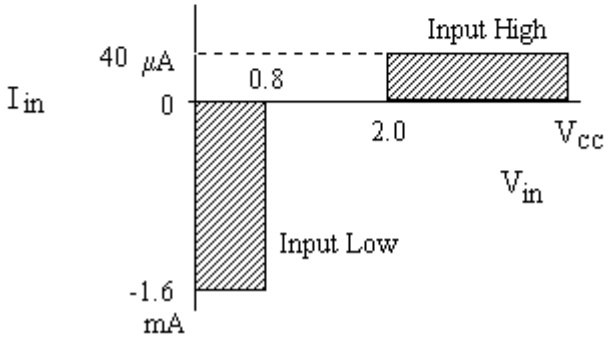
You will note in the above examples that there is no mathematical relationship between one variable and another. There is simply not enough data to develop one and the variability of the manufacturing process prohibits the manufacturer from providing one.

In a design setting, you must stay within the limits provided by the manufacturer. For example, if you wanted to connect a resistor from the output of a 7400 gate and ground, what would be the limits allowed on the resistance value? Figure 10c provides part of the answer. If we assume that we must operate within the shaded region which represents a "High" level output, we should not allow the output to drop below 2.4 volts with 400 μA coming out of the gate. The minimum value would be 6 KΩ. The upper limit is, of course, infinite; an open circuit ($V_o = V_{CC}$, $I_o = 0$).

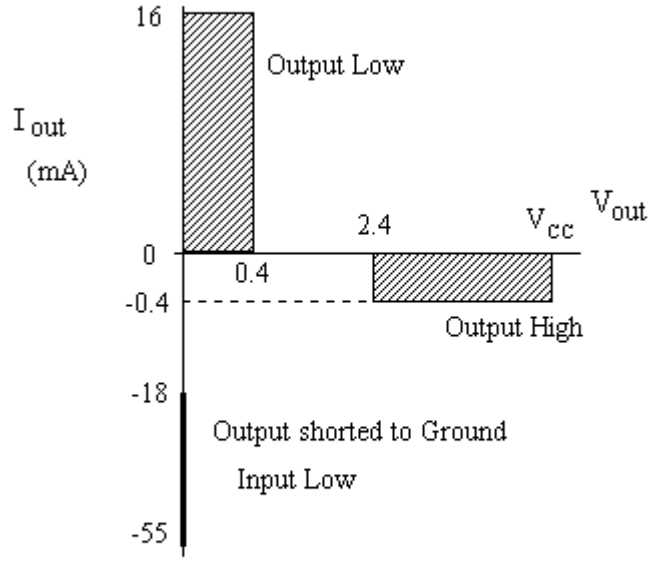
There are a few data points provide by the specifications that are not within the limits of normal operation. For example, if the input voltage drops below zero, it is allowed to drop to -1.5 volts where you may expect as much as 12 mA coming out of a 7400 gate input. Most of this current comes from an input clamp diode which has not been shown on our drawings.



a. Allowed operating region, V_{out} vs V_{in}, for a 7400 gate.



b. Allowed operating region, I_{in} vs V_{in}



c. Allowed operating region, I_{out} vs V_{out}

Figure 10. Allowed operating regions for a 7400 gate.

Another non-standard data point of interest is I_{oS}, the short-circuit output current. This is the current you get from the gate output if the output is shorted to ground when the output of the gate would otherwise be high. In this case, both minimum and maximum values are given, -18 to -55 mA. If you went to the laboratory and actually performed this deed, you could expect a current somewhere in this range. How does this affect the designer? For example, a designer might be tempted to connect the output of the 7400 gate directly to the base of an NPN transistor whose emitter is grounded. In this case, the "high" output voltage is clamped at 0.80 V by the BE junction. What current can you expect into the base of the transistor when the gate output goes "high"? This condition is tricky and perhaps open to some debate, but the conservative designer must recognize that the operation is between the short circuit case and the case where V_{oHmin}=2.4V when I_{oH} =-400μA. The conservative designer would conclude that the current might be as low as 400 μA and as high as 55 mA; the worst cases. It is possible to go back to the circuit of the gate with 0.8 volts at the output terminal and calculate the current. However, this analysis would be for nominal values only and not provide definitive limits on the current.

Note the notation at the bottom of the specification table in Figure 9. This notation discusses the limit on the amount of time a short circuit is allowed to be connected to the output of some gates. This time limit is based on the amount of time it takes the internal components of the integrated circuit to heat up to its maximum allowed value. While connecting a transistor base to the output is not exactly a short circuit, it is outside the allowed operating region and probably should have the same time limits as the short circuit.

TERMINAL CHARACTERISTICS

During the previous discussions on TTL, we were looking at circuit operation and developing an understanding of how the terminal specifications were arrived at. Let us now take a broader look at these characteristics.

First, the input currents are quite high when the input is low, requiring the driver to **sink** a lot of current. When the input is high, the input current into the gate is quite low. Thus, any circuit which is supposed to drive the input to a TTL gate must concentrate on sinking current, and only needs to source a little current when the driver output voltage is high.

Second, the output strength of the TTL gate matches the strength requirements at the input. An example is given in Figure 11. The TTL gate can sink a large current when its output is low, but can only source a small current when the output is high. Thus, if the TTL gate is expected to drive a circuit that is not another TTL circuit, you must exercise care when designing the interface. The load circuit must not require large input currents when its input is high, but may use larger currents when the input voltage is low.

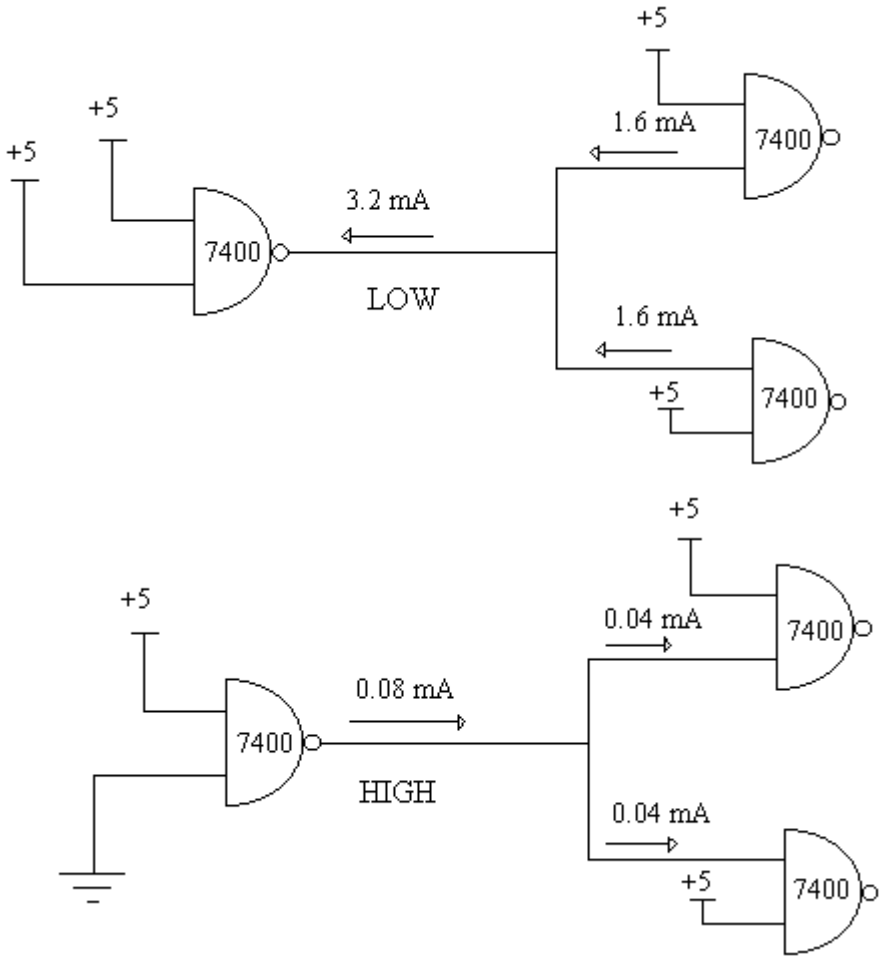


Figure 11. When driving other TTL gates as loads, a 7400 gate must be able to sink more current than it needs to source.

These requirements must be kept in mind when designing interfaces with the TTL gate at both the input and the output. Examples of interfacing with TTL gates are shown in Figure 12 and 13. See data books for more complete data.

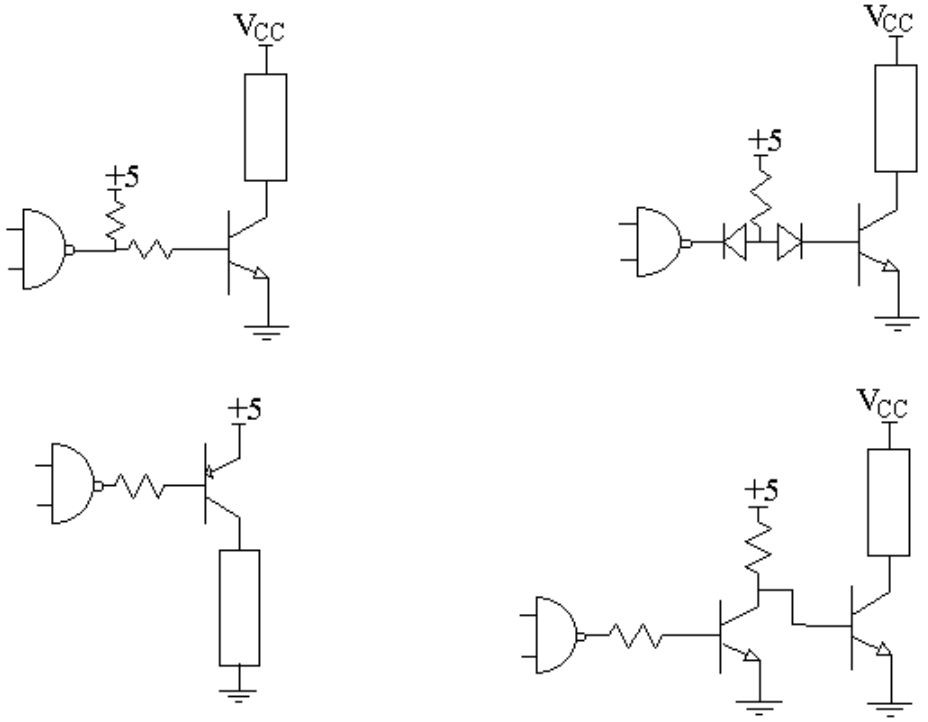


Figure 12. Several ways to drive loads from TTL gates.

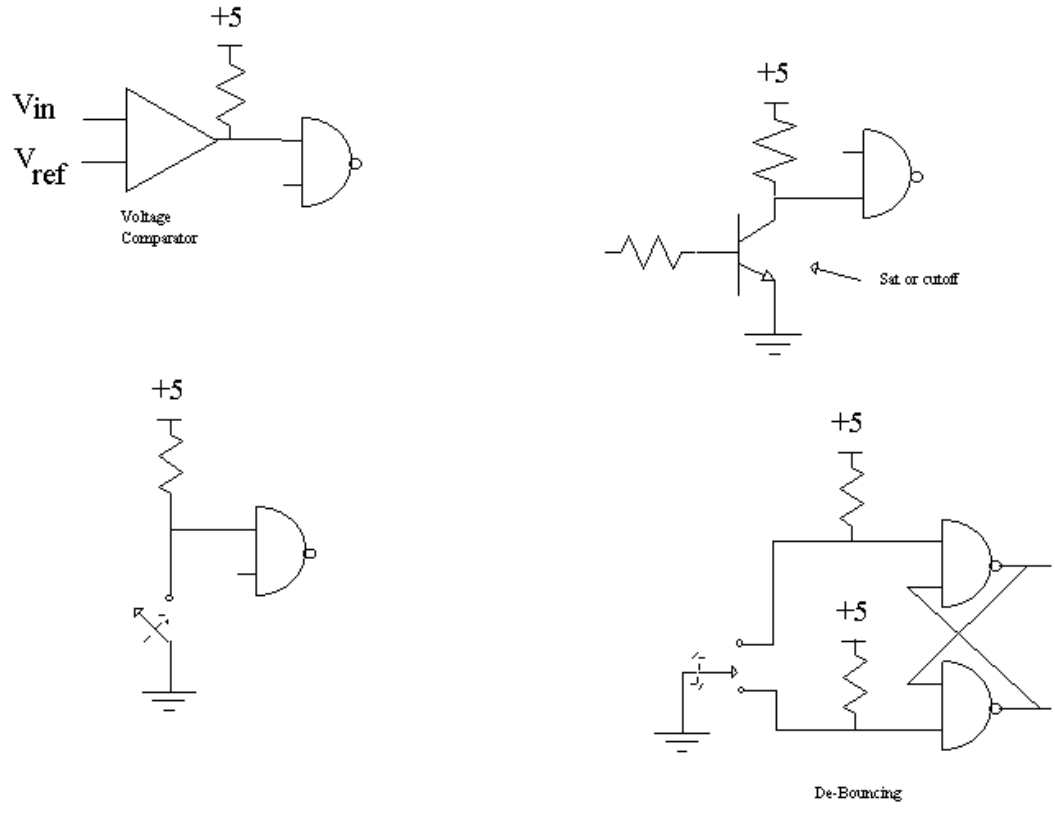


Figure 13. Several interfaces to drive TTL gates.

WIRED-AND CONNECTION

Because the active pull-up or totem-pole output of the TTL gate always has one transistor cutoff and the other turned on, you cannot connect two outputs together. If one is trying to pull the output high, and the other is trying to pull it low, you will have a very low impedance path to ground and very large currents.

For the same reason, the output must not be connected to any voltage source or to ground through a low impedance path. In one state or the other, there would be a low impedance path and large currents.

OPEN COLLECTOR GATES

In order to overcome the limitations created by the totem pole output circuit, some gates are manufactured with the output collector left open. One example is the 7405, a quad 2-input NAND gate with open collector outputs. If you connect a resistor as the pull-up, you can use this resistor to source current when the output is high and/or you can wire-AND the collectors together.

TTL FAMILIES

As the designers of TTL gates became more sophisticated, they developed modifications which would provide special characteristics. The original series of TTL was designated as 74XX, where the XX is replaced by logic function (00 is a quadruple 2-input NAND, 04 is a hex inverter, etc.) The 74LXX series is a low power family. 74HXX is a high speed family. 74SXX is a family based on Schottky diodes and transistors. 74LSXX is a family of low power Schottky. A 54xXX is also provided as a companion family to the 74xXX families. The 54... families are identical to the 74... families, except for operating temperature range and tolerance on power supply voltage.

Each family has different characteristics, but the same logic functions. The L family is low power, but is much slower than the standard family. The H family is high speed, but also has higher power dissipation. The Schottky families are quite fast without increasing the power dissipation. More recent advances in TTL family have given us several other versions. For example, 74F, 74AS, and 74ALS, for Fast, Advanced Schottky, and Advanced Low-power Schottky. The AS family is the fastest, with a propagation delay of less than 5 ns. Table 2 shows the propagation delays and power supply current for each type of gate. The power supply current, I_{CC}, is the average for a 50% duty cycle with the output spending half its time low and half the time at a high.

In addition, these different families use slightly different circuit configurations. A little study of the circuits will reveal the same operations.

Table 2. Propagation delays and power supply current for TTL families
Data abstracted from Texas Instruments TTL Data Books

Gate	t_{PLH} (ns)			t_{PHL} (ns)			I_{CC} (mA)
	min	typ	max	min	typ	max	typical
7400		11	22		7	15	2.00
74L00		35	60		31	60	0.20
74H00		5.9	10		6.2	10	4.50
74LS00		9	20		10	20	0.40
74S00	2	3	4.5	2	3	5	3.75
74ALS00	3		11	2		8	1.00
74AS00	1		5	1		4	6.20

SCHOTTKY TTL

A Schottky PN junction is made up of a semiconductor and a metal. This kind of junction has two characteristics: low turn-on voltage and low junction capacitance.

When a Schottky junction is used in place of or in parallel to the Base-Collector junction of a transistor, the transistor is faster because of the lower junction capacitance and because the transistor cannot go so deep into saturation. Because the turn-on voltage for the BC junction is lower, V_{CEsat} is higher.

Schottky TTL is thus faster than standard TTL and the terminal voltages are slightly different. See the data sheet.

TRI-STATE OUTPUT

The totem-pole output of a TTL gate provides additional speed at lower power for the gate than a simple pull-up resistor. The cost, however, is that the gate outputs cannot be connected in parallel. This problem is serious when you need to make a bus structure such as a data bus, where several gates need to put data onto the bus at different times. The outputs can be OR'd or AND'ed using appropriate gates, but this solution is less than satisfactory and slows down the operation.

A better solution is the TRI-STATE output as shown in Figure 14. The added input allows normal operation of the gate when the "enable" input is high. Both output transistors are cutoff when "enable" is low.

Resistor-Transistor Logic

Resistor-transistor logic, RTL, is an old technology that is no longer commercially available. It is a useful starting place to study logic gates because it is a logical extension of the transistor inverter studied in the previous chapter, and because it is a useful circuit in itself.

A two-input gate is shown in Figure 1. As with most logic, the transistors operate only in saturation or cutoff. There are four possible combinations of logic inputs, L-L, L-H, H-L, and H-H for inputs A and B respectively. A low input will cutoff the associated transistor, and a high input will saturate it. Figure 2 shows these combinations where the transistors have been replaced by their corresponding models. If both transistors are cutoff, the output will be high, 3.0 Volts. If either transistor is saturated, the output will be 0.2 Volts, or low. The truth table for this gate is given in Figure 3 and shows that the gate performs a logic NOR function.

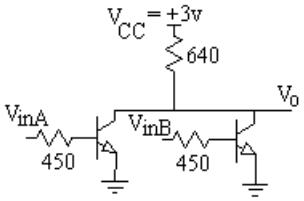
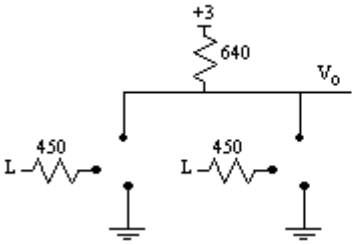


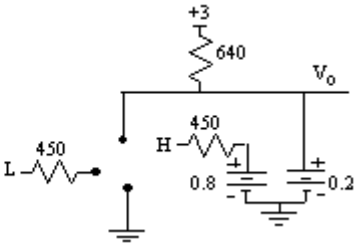
Figure 1. RTL gate

V_{inA}	V_{inB}	V_o
L	L	H
L	H	L
H	L	L
H	H	L

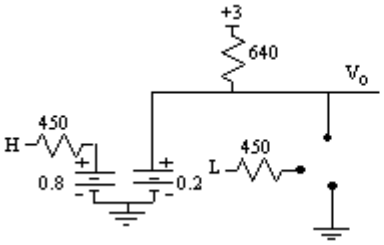
Figure 3. Truth table for RTL gate



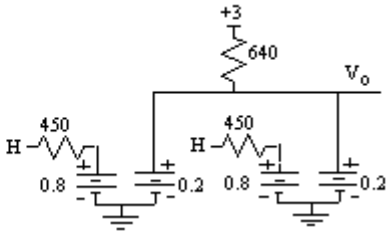
a. L-L inputs



b. L-H inputs



c. H-L inputs



d. H-H inputs

Figure 2. RTL gate with four combinations of inputs

Our job is to determine the eight terminal specifications, input and output voltages and currents when these terminals are both high and low as shown in Table 1. Definitions of these terms are given in Appendix A.

Table 1. The Eight Terminal Specifications to be Determined.

V_{inH}	V_{inL}	I_{inH}	I_{inL}
V_{oH}	V_{oL}	I_{oH}	I_{oL}

We begin the calculation of the terminal specification by noting that when a transistor is saturated, the collector-emitter voltage is 0.2 volts. The output terminal is connected directly to the collector terminal, thus, $V_{oL} = 0.2$ volts. Assume the gate on which this analysis is taking place is embedded in a logic system. Its inputs are driven by other identical logic gates. Then if the outputs of those driver gates are logic low, the inputs to the device under analysis are low. We will use this as a starting place for the calculations.

$V_{inL} = 0.2$, (LOW input to both transistors)

Under this condition, both transistors will be cutoff, making the output high. The circuit diagram with circuit models for the cutoff transistors is shown in Figure 4. The output voltage then is 3.0 Volts. We will call this a no-load condition when there is no load connected to the output.

$V_{oH} = 3.0$ Volts (No-Load)

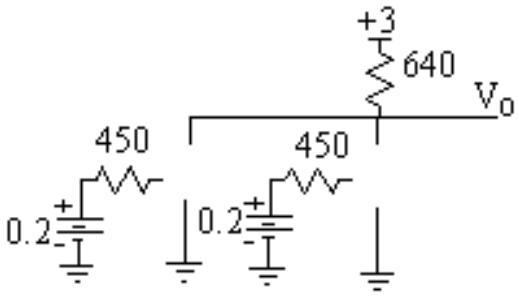


Figure 4. RTL gate with both inputs low. The transistors are replaced by the cutoff model.

Also note from Figure 4 that the input current is zero because the transistor is cutoff. Thus,

$$I_{inL} = 0$$

The question naturally arises about how high the input voltage may rise and still keep the transistor cut off. The input voltage must stay below $V_{BE\gamma}$ to guarantee the transistor is off, making

V_{inLmax} = 0.5 Volts.

The maximum value is given in this case because we need to know how high it may rise. This means that the input voltage may rise as high as 0.5 volts and still keep the transistors off, and will always be recognized by the gate as a "low".

INPUT HIGH

In this case we want the transistor to be saturated. Either transistor saturated will cause the output to go low, to 0.2 volts. This case is shown in Figure 5. We show the circuit with one of the transistors cutoff, although both saturated would produce the same result. We start by determining the minimum input current that will keep the transistor in saturation.

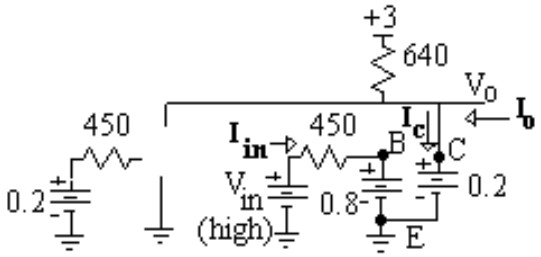


Figure 5. RTL gate with one input high.

$$I_{Csat} = \frac{3.0 - 0.2}{0.640k} = 4.375mA$$

The minimum base current to keep the transistor saturated is (assuming β=30)

$$I_{inH\min} = \frac{I_{Csat}}{\beta} = \frac{4.375}{30} = 0.146mA$$

The minimum value is of interest because this current is dependent on the input voltage. From this value, we can determine the minimum input voltage that will be guaranteed to be recognized as a "high".

V_{inHmin} = 0.8 + 0.146 mA x 0.450 KΩ = 0.866 Volts

Any input voltage greater than or equal to 0.866 volts will cause the transistor to be saturated, and thus be recognized as a "high". We previously found V_{inLmax} =0.5 volts. Any input voltage between 0.5 and 0.866 is an invalid logic level and the manufacturer assumes no responsibility if you provide an input voltage in that range. For the gate with no load, the relationships between input and output voltages are presented graphically in Figure 6. The noise margins NMH and NML are defined in Appendix B.

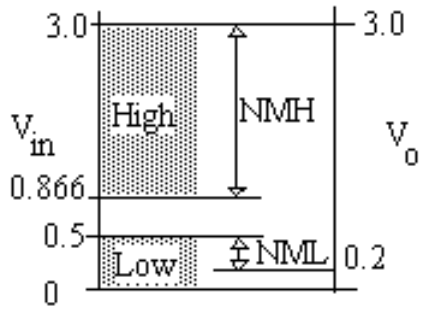


Figure 6. Graphical representation of input voltage ranges and output voltages for the unloaded RTL gate.

CALCULATIONS WHEN THE GATE IS USED TO DRIVE OTHER GATES

Up to this point we have done all calculations assuming no load on the gate. While convenient for visualization, it is not a very useful situation. Let us look at the loading of the gate as if it were embedded in a logic system driving identical gates as shown in Fig. 7.

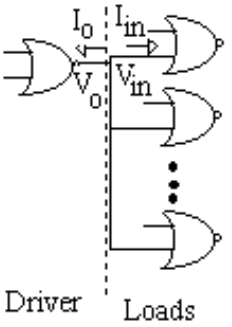


Figure 7. Driver gate being analyzed driving load gates.

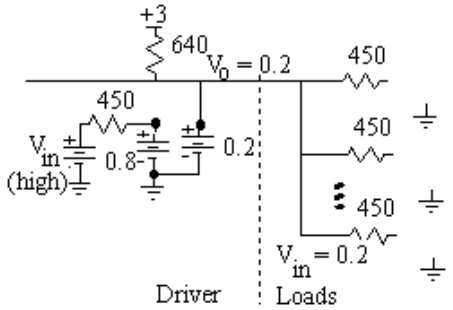


Figure 8. Driver with loads when driver output is low.

There are two cases, the driver output being low as shown in Figure 8, and the driver output being high as shown in Figure 9. When the output is low, the driver transistor is saturated and the output is 0.2 Volts. All the input transistors of the load gates are cutoff and no current flows. The output voltage remains at 0.2 volts, unchanged by the loads.

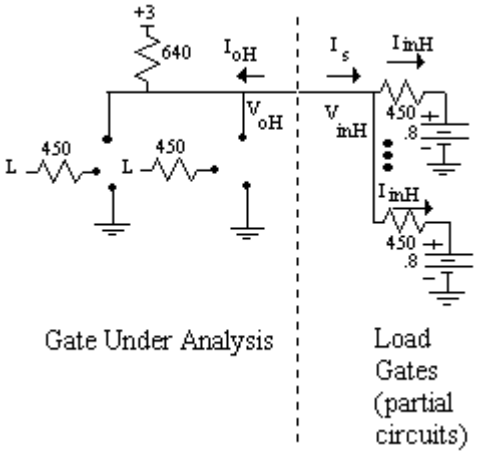


Figure 9. RTL gate with N loads when driver output is high.

However, when the output is high, the load gates require current, pulling the output voltage down. This situation is shown in Figure 9 with an unspecified number of loads. How many can you connect and still expect the gates to work right? This is called the maximum fanout. The output voltage is determined by the load current being SOURCED by the driver.

$V_{oH} = 3.0 - I_S \times 0.64\ k\Omega$

Where the current coming out of the driver gate is divided between the load gate inputs. Since the minimum voltage at the load gate inputs when high is 0.866 Volts, this is the lowest the output voltage of the driver gate may go. Thus,

$$I_{oH\max} = -\frac{3.0 - 0.866}{0.64k} = -3.334mA$$

The negative sign comes about because currents are always defined as positive when going into the terminal. Each load requires a minimum of 0.146 mA as input current, therefore, the maximum fanout is

$$MaxFanout \le \frac{3.334}{0.146} = 22.8$$

Thus, the maximum fanout is 22.

PRACTICAL FANOUT

The maximum fanout will not provide for any noise margin. Also, manufacturing tolerances will not allow such close calculations. Therefore, most manufacturers limit the allowed fanout to a much smaller number than found by nominal and typical calculations. Typically, the fanout would be limited to say 5 loads. In this case, the output voltage under maximum load would be substantially higher than calculated above. With five loads, the output current will be

$$I_{oH} = -\frac{3.0 - 0.8}{0.64 + \frac{0.45}{5}} = -3.014mA$$

and the output voltage will be

$V_{oH} = 3.0 - I_{oH} \times R_c = 3.0 - 3.014 \text{ mA} \times .64 \text{ k}\Omega = 1.071 \text{ Volts}$

Under this condition, the Noise Margin High is

NMH = 1.071 - 0.866 = 0.205 Volts

Note that in many cases the output voltage will be higher than the value just calculated and thus the noise margin larger. If we define the maximum allowed fanout to be five, then $V_{oHmin} = 1.071$ Volts.

CALCULATION OF I_{oL}

If we define the maximum allowed fanout to be five, then the minimum voltage ever seen by the input will be 1.071 Volts. The minimum current into the input will be

$$I_{inH\min} = \frac{1.071 - 0.8}{0.45k} = 0.602mA$$

The maximum collector current is β times this or 18.067 mA and still stay in saturation. Thus, the maximum output current when the output is low is this current minus the current down through the 640 Ω resistor.

$I_{oLmax} = 18.067 - 4.375 = 13.692 \text{ mA}$

We now have all the specifications for this gate. The results are shown in Table 2. We have assumed here that the fanout is limited to 5 loads. There is a certain amount of arbitrariness in the choice of V_{oH} and I_{oH}. Many other performance requirements could have been chosen. The values given are self consistent, however. First note that $V_{oHmin} > V_{inHmin}$ and $V_{oLmax} < V_{inLmax}$, as shown in Figure 10. The voltages are compatible.

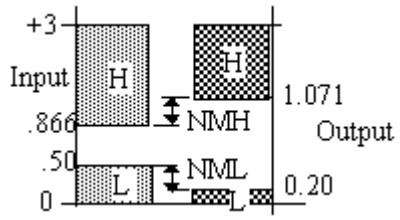


Figure 10. Voltage compatibility chart, with 5 loads

To determine fanout,

$$\frac{I_{oH}}{I_{inH}} = 5.007 \quad \text{and} \quad \frac{I_{oL}}{I_{inL}} = \infty$$

Therefore, the fanout is 5.

Table 2. Terminal specifications for the RTL Gate

V_{inLmax} = 0.500 Volts V_{oL} = 0.2 Volts

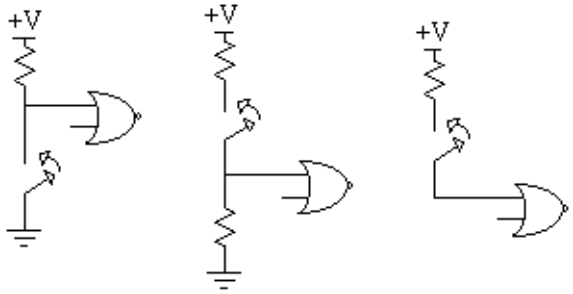
V_{inHmin} = 0.866 Volts V_{oHmin} = 1.071 Volts (N=5)

I_{inL} = 0 I_{oLmax} = 13.692 mA ($V_{in} > V_{oHmin}$)

I_{inHmin} = 0.602 mA I_{oHmax} = - 3.014 mA

INTERFACING TO RTL

Table 2 is a set of specifications that would be provided by the manufacturer of the RTL logic. From this information, you would be expected to be able to use the gates without exceeding any specification. Any gate embedded in a logic system using only the RTL gates analyzed, would be guaranteed to work within the specifications. The only limitation we must follow is limiting the fanout to five loads. However, logic is rarely used without interfacing to the outside world at some point. There must be some signals at some point that are generated outside the logic system that must be recognized as a logic one or a zero. Similarly, there is usually some point where a logic gate output must drive a device that is not another gate.



a. b. c.

Figure 11. Three possible configurations of a switch-to-logic gate interface.

Figure 11 shows three possible connection using a switch to generate the logic inputs to a gate. In Figure 11a the switch is used as a pull-down to make the input voltage a logic zero when the switch is closed. The resistor pulls the input voltage up to a logic one when the switch is open. Looking at the specifications in Table 2, we note that when the switch is closed, the input voltage is zero volts, well below the required V_{inLmax} of 0.5 volts. The gate input current is zero so the switch needs only to handle the current coming down through the resistor. When the switch is open, current will come down through the resistor into the gate input terminal. The specifications show the voltage must be above 0.866 volts and the current must be at least 0.602 mA. From these values, we can select a value of R_1. To provide a noise margin, we should certainly provide a voltage at least as high as V_{oHmin} = 1.071 volts. Let's shoot for 2.0 volts to provide even greater noise margin. We know this will provide greater than the minimum current, but we don't yet know how much. We now have to put on our engineer's hat and look inside the gate to finish the design. The parts of the circuit that pertain to this case are shown in Figure 12 with only the base-emitter voltage of the transistor shown. The transistor must be in saturation so we use 0.8 volts for V_{BEsat}.

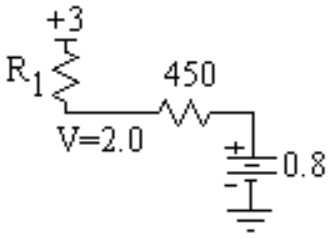


Figure 12. Circuit with switch open.

Solving this circuit, we can write a single node equation at the input node, V_{in} = 2.0 v,

$$(3.0-2.0)/R_1 = (2.0-0.8)/450$$

Solving, we get R_1 = 375 Ω. This is not a standard resistor value so we would select a nearby standard value and re-solve the circuit, this time to determine the input voltage. If we are satisfied with the result, then we are finished. If the input voltage found is not satisfactory, we would try with another value. Note that we do not have to get 2.0 volts, we simply chose that value as a place to start the design. We do, however, have to provide $V_{in} > V_{inHmin}$.

The design of the circuit in Figure 11b would follow a similar track. Notice that in this circuit the input voltage is high when the switch is closed; the opposite of the circuit in Figure 11a. Figure 11c is simpler than 11b, but it is not recommended because when the switch is open, the input lead of the gate is floating or disconnected and susceptible to noise which might cause random errors in the logic.

Figure 13 shows an example of an interface at the output of the gate. In this case, we want to drive an LED at 30 mA. Neither the high nor low output currents of the gate are sufficient, so we use a transistor as a current amplifier. Many other configurations are possible and some may be preferrable depending on the application. We will not go through the design of this circuit here. A similar circuit was designed at the end of the previous chapter.

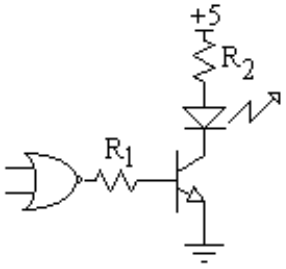


Figure 13. Example of an output interface circuit.

EMITTER-COUPLED LOGIC

The major speed limitation of TTL is the turn-off time of saturated transistors. To be sure, TTL has come a long way from the 100 ns time of DTL to the 2-4 ns propagation delays of ASTTL. ECL is designed so that the transistors are either cutoff or in the active region, rather than cutoff or saturation for the DTL/TTL. With the transistors in the active region, the charge stored in the base region of the transistors is kept to a minimum, allowing shorter turn-off times. Typical propagation delays of "standard" ECL are about 1 ns, and down to about 0.5 ns for some of the advanced types.

There are several disadvantages associated with ECL. It uses a negative power supply so that the logic levels are not compatible with any other logic family, and makes analysis and measurement inconvenient. ECL requires large currents and the noise margins are small. On the other hand, power supply currents remain much more stable when the logic switches compared to TTL, thus reducing noise on the power leads. In practice, ECL is used only when necessary for its high speed. ECL has been around since the early 60's, being developed at about the same time as DTL.

Before we start the analysis of the circuit, we need to look at the circuit model we will use for the transistors in the ECL circuit. Because ECL is predicated on speed, the size of the transistors is as small as possible to keep stored charge to a minimum. Thus, current densities and hence, voltage drops will be slightly higher than normal. For this reason, we will use different voltages for base-emitter voltage for ECL.

$V_{BE\gamma} = 0.65$ and $V_{BEactive} = 0.75$ volts

ECL is based on the emitter coupled pair shown in Figure 1. This pair will have one transistor on and the other cutoff in each logic state. If we compare the currents through the two transistors, one with 0.75 volts between base and emitter and the other with 0.65 volts, we will find that the transistor with the higher voltage will be carrying nearly 50 times the current of the other. Thus, the lower voltage transistor will essentially be cutoff.

$$\frac{I_{B1}}{I_{B2}} = \frac{I_o e^{\frac{0.75}{V_T}}}{I_o e^{\frac{0.65}{V_T}}} = 47.5 \qquad \text{where } V_T = 25.9 \text{ mV}$$

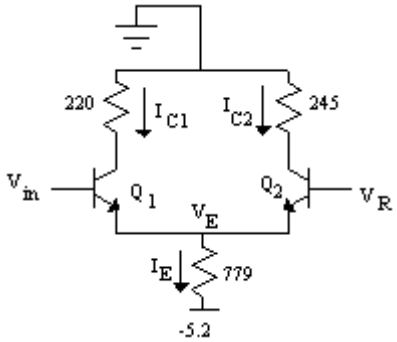


Figure 1. Emitter coupled Pair

BASIC OPERATION OF THE EMITTER-COUPLED PAIR

We start by looking at the operation of the difference amplifier shown in Figure 1. The two transistors are connected at their emitters. The base of Q_2 is connected to a reference voltage, V_R.

Consider for an example, that the input voltage is low enough to keep Q_1 cutoff. Then, Q_2 will be conducting and the emitter voltage will be

$$V_E = V_R - V_{BEon} = V_R - 0.75$$

assuming Q_2 is operating in the active region. We know Q_2 is in the active region because the collector resistors are selected to keep the transistors from saturating.

How high can we raise the input voltage and still keep Q_1 off?

$$V_{inLmax} = V_E + V_{BE\gamma} = V_R - 0.75 + 0.65 = V_R - 0.10 \text{ volts}$$

Now, let the input voltage start rising above this voltage. Then Q_1 begins to turn on. This increases the current through R_E, raising the voltage at the emitters. This voltage rise causes Q_2 to begin to turn off. The input voltage rises only a little bit before Q_2 turns off entirely. The minimum high level input voltage occurs when $V_E = V_R - 0.65$ and

$$V_{inHmin} = V_E + 0.75 = V_R + 0.10 \text{ volts}$$

Thus, a 200 mV swing at the input causes a complete reversal in which transistor is turned on and which is turned off.

ANALYSIS OF THE ECL GATE

We now turn our attention to Figure 2, the complete ECL gate circuit. In this circuit we have added two emitter follower output stages. As we shall see later, these output stages serve the purposes of buffering the gate output, providing added fanout, as well as shifting the voltage levels.

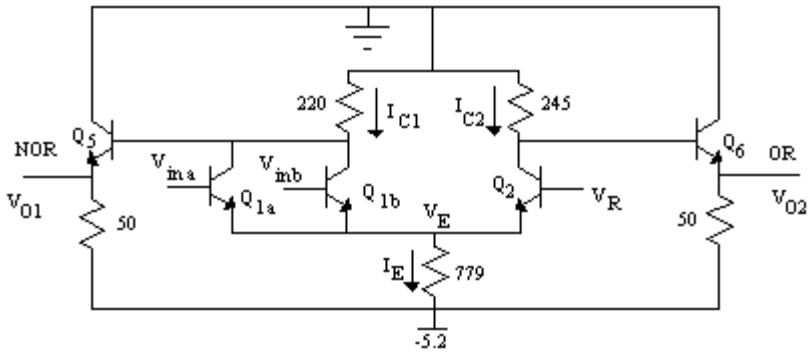


Figure 2. Complete ECL Gate

OR OUTPUT --- Output high, Q_2 off
With Q_2 off, the output circuit looks like that shown in Figure 3.

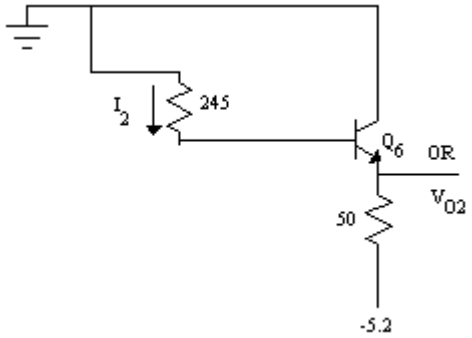


Figure 3. Equivalent Circuit With Q_2 OFF.

If we assume a very high β, we can ignore base current ($I_2 \cong 0$) but the transistor Q_6 is in the active region so

$V_{oH} = V_{o2} \cong -0.75$ volts

(Note that since the collector is at 0V, and the emitter is at -0.75V, the transistor is in the active region. This type of circuit is called an emitter follower. The output voltage is always $V_{BEactive}$ below the base voltage and follows the base voltage, even when the output goes low as we shall see next.)

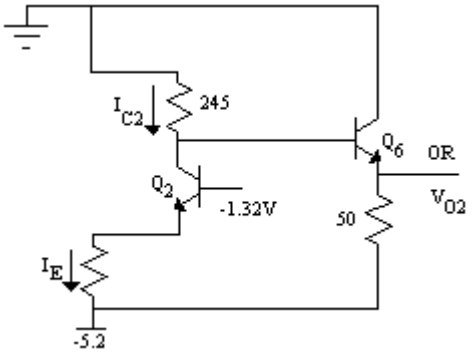


Figure 4. Equivalent Circuit With Q_2 ON.

OR OUTPUT LOW - Q_2 ON, Q_1 OFF,

The circuit for this case is shown in Figure 4. The emitter voltage is:

$V_E = V_R - 0.75 = -2.07$ volts

Thus, the current down through the emitter resistor is

$$I_E = \frac{-2.07 - (-5.2)}{779} = \frac{3.13}{779} = 4.018mA$$

If we assume β is very large so base currents can be neglected, the collector current in Q_2 will be the same as the emitter current. Thus, the voltage at the collector of Q_2 (and the base of Q_6) will be

$V_{C2} = V_{B6} = -I_{C2}*245 = -0.98$ (Note that $V_{C2} - V_E = 1.09$v. Q_2 is in active region.)

Thus, the voltage at the emitter of Q_6 will be

$V_{oL} = V_{o2} = -0.98 - 0.75 = -1.73$ volts

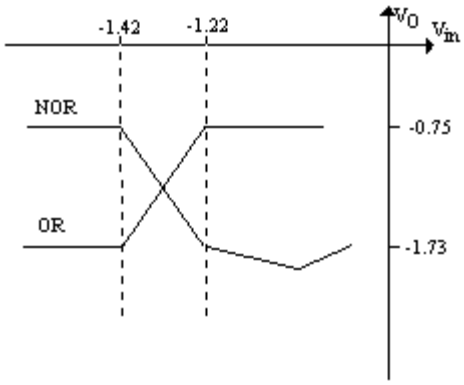
We can now plot the output at V_{o2} versus the input voltage. The result is shown in Figure 5.

NOR OUTPUT, Q_1 OFF, Output High

This case is essentially the same as for the OR output when it is high, except that we have a 220 Ω resistor instead of a 245 Ω resistor at the collector. Again, because the base current is so small, the output voltage will be -0.75 volts, the same as for the OR output.

NOR OUTPUT, Q_1 ON, Q_2 OFF, Output Low.

This case is similar to the OR output high case, except that the input voltage can directly affect the collector current through Q_1 causing the voltage at the base of Q_1 to change. As V_{in} increases, the current increases causing the voltage at the base of Q_5 to decrease. Because the output follows the base voltage with a 0.75 volt difference, the output drops as V_{in} increases. This scenario holds until Q_1 saturates. Then as V_{in} increases further, the base-collector junction is forward biased, and current flows from the input toward the collector, raising the voltage at the base of Q_5, hence raising the output voltage. The resulting plot of V_{o1} vs V_{in} is also shown in Figure 5.


-1.42
-1.22
V_O
V_{in}
NOR
OR
-0.75
-1.73