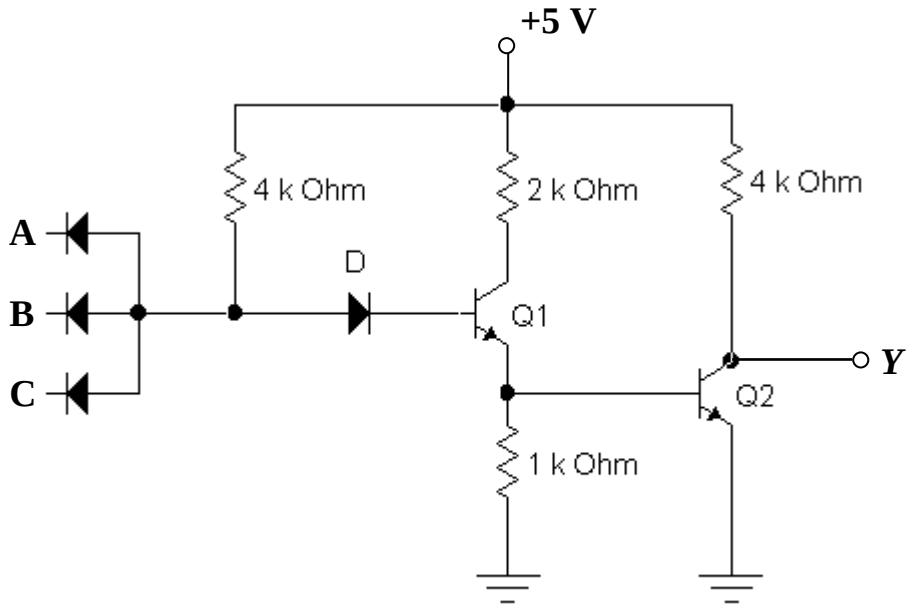
Questions for Training

Q1) For the circuit shown in figure below:

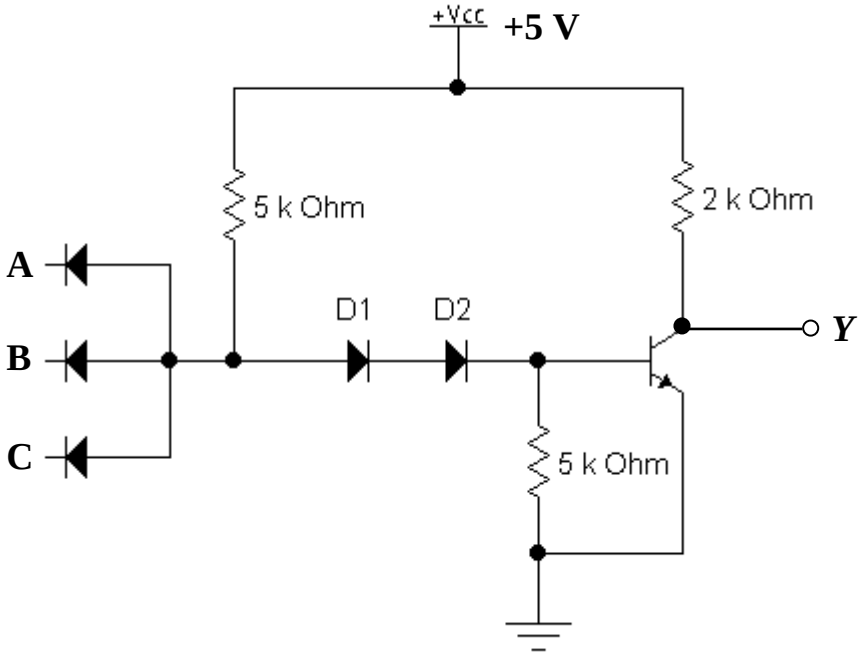
I) Verify that $Y = \overline{ABC}$..

II)Determine the Fan-Out.

Assume $\beta_{min.}$=25, $V_{BEsat.}$=0.8V, $V_{CEsat.}$=0.2V, & V_{BE}=0.7V.



Q2) Show that the output transistor of the ***DTL*** gate of figure below goes into saturation when all inputs are ***HIGH***. Assume that h_{FE}=20, V_{BE}=0.7V, $V_{BEsat.}$=0.8V, & $V_{CEsat.}$=0.2V.

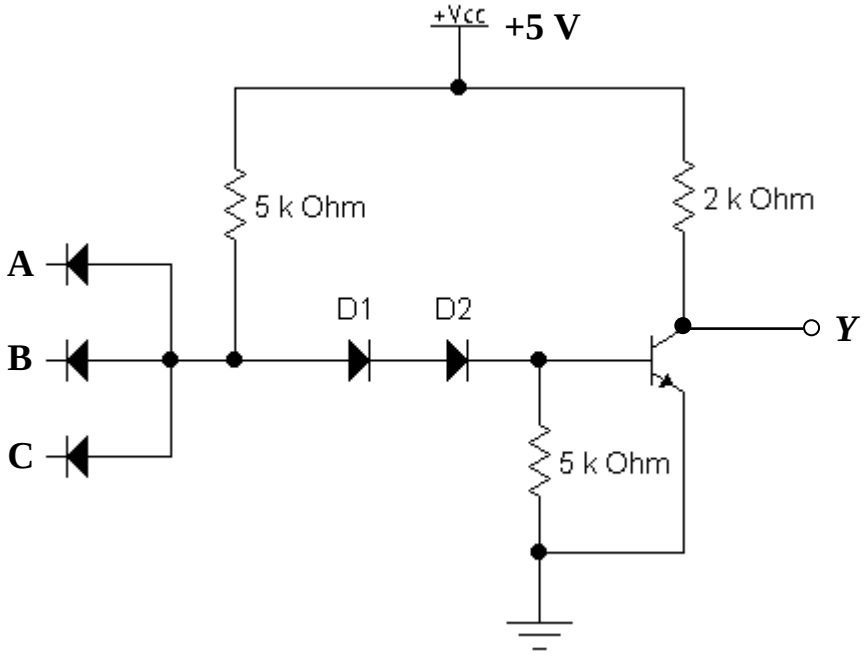


Q3) Connect the output ***Y*** of the ***DTL*** gate shown in figure below to ***N*** inputs of other similar gates. Assume that the output transistor is saturated. Let h_{FE}=20, V_{BE}=0.7V, $V_{BEsat.}$=0.8V, & $V_{CEsat.}$=0.2V.

I) Calculate the current in the ***2kΩ*** resistor.

II) Calculate the current coming from each input connected to the gate.

III) What is the Fan-Out of the gate?



Q4) For the NAND gate shown in figure below. Determine the Fan-Out and calculate the average power dissipated by the gate. Assume $\beta_{min.}$=25, $V_{BEsat.}$=0.8V, $V_{CEsat.}$=0.2V, & V_{BE}=0.7V.