DIGITAL COUNTER AND APPLICATIONS

A **digital counter** is a device that generates binary numbers in a specified count sequence. The counter progresses through the specified sequence of numbers when triggered by an incoming clock waveform, and it advances from one number to the next only on a clock pulse. The counter cycles through the same sequence of numbers continuously so long as there is an ***incoming clock pulse***.

The binary number sequence generated by the digital counter can be used in logic systems to *count up or down*, to generate truth table input variable sequences for logic circuits, to cycle through addresses of memories in microprocessor applications, to generate waveforms of specific patterns and frequencies, and to activate other logic circuits in a complex process.

Two common types of counters are **decade counters** and **binary counters.** A decade counter counts a sequence of *ten numbers*, ranging from 0 to 9. The counter generates four output bits whose logic levels correspond to the number in the count sequence. Figure (1) shows the output waveforms of a decade counter.

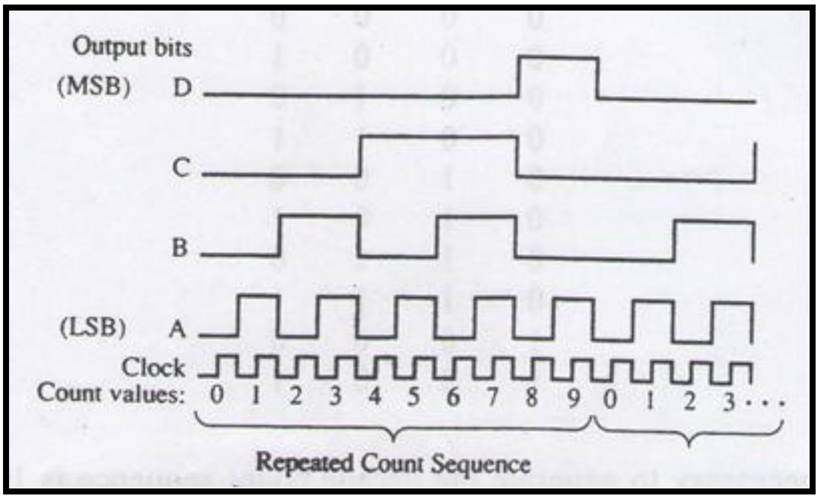

Figure (1): Decade Counter Output Waveforms.

A binary counter counts a sequence of binary numbers. A binary counter with four output bits counts 2^4 or 16 numbers in its sequence, ranging from 0 to 15. Figure (2) shows-the output waveforms of a 4-bit binary counter.

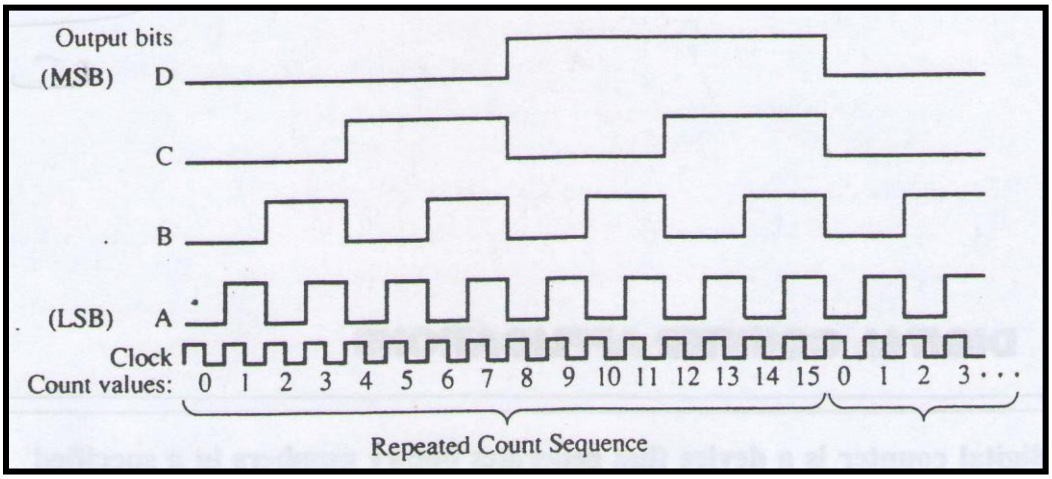

Figure (2): Binary Counter Output Waveforms.

EXAMPLE (1): Decade Counter.

Problem: Determine the 4-bit decade counter output that corresponds to the waveforms shown in Figure (1). Determine the time required for the counter to generate the entire count sequence if the input clock has a period of 1 ms.

Solution: The count sequence generated by the decade counter whose waveforms are shown in Figure (1) is listed here:

The time necessary to generate the decade count sequence is 10 ms if the input clock has a 1 ms period.

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

EXAMPLE (2): Four Bit Binary Counter.

Problem: Determine the 4 bit output that corresponds to the output waveforms shown in Figure (2).

Solution: The 4-bit output generated by the waveforms in Figure (2) is listed here.

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

EXAMPLE (3): Four Bit Binary Counter.

Problem: Determine the period and frequency of each output waveform shown in Figure (2) if the input clock has a period of 1 ms.

Solution: A output: Period = 2 ms, frequency = 500 Hz.

B output: Period = 4 ms, frequency = 250 Hz.

C output: Period = 8 ms, frequency = 125 Hz.

D output: Period = 16 ms, frequency = 62.5 Hz.

Section Self-Test

1. What is a decade counter?

2. What is a binary counter?

3. What relationship is there between the frequency outputs from each bit of a binary counter?

ANSWERS: (Not necessarily in the order of the questions).

- The frequency of the least significant bit is one half the clock frequencies. The frequency of each bit is one half the frequency of the previous output.
- Counts binary numbers in a sequence, either up or down. For a binary counter with n bits, there are 2n count values in the sequence.
- Counts a sequence of ten values.

COUNTER CLASSIFICATION

Digital logic counters can be classified according to their operational characteristics. The key characteristics that must be determined through analyzing the counter circuit are the count modulus, counter stages, output bits, frequency division, asynchronous operation, synchronous operation, and trigger characteristics, as described in sections below.

1. Count Modulus

The count modulus is the total number of **states** or values generated by the counter as it progresses through its specified sequence. The modulus, or **MOD,** is one of the most important characteristics to specify when classifying a counter since it identifies the number of values in the count sequence and determines the frequency division capabilities of the counter. **Decade** counters always have a **modulus** of **10** and are sometimes referred to as **MOD-10 counters. Binary** counters of n bits have a **modulus of** $\mathbf{2^n}$.

Figures (1 and 2) show that the modulus of a counter can be determined by a waveform generated by the counter. A count modulus can also be designated by a

state transition diagram. The states of a counter are the output numbers generated by the counter. A state transition diagram shows the progression of the number generated from one clock pulse to the next. The total number of states in the diagram is the modulus of the counter. Figure (3) shows the state transition diagrams for the decade counter and binary counter whose waveforms were shown in Figures (1 & 2).

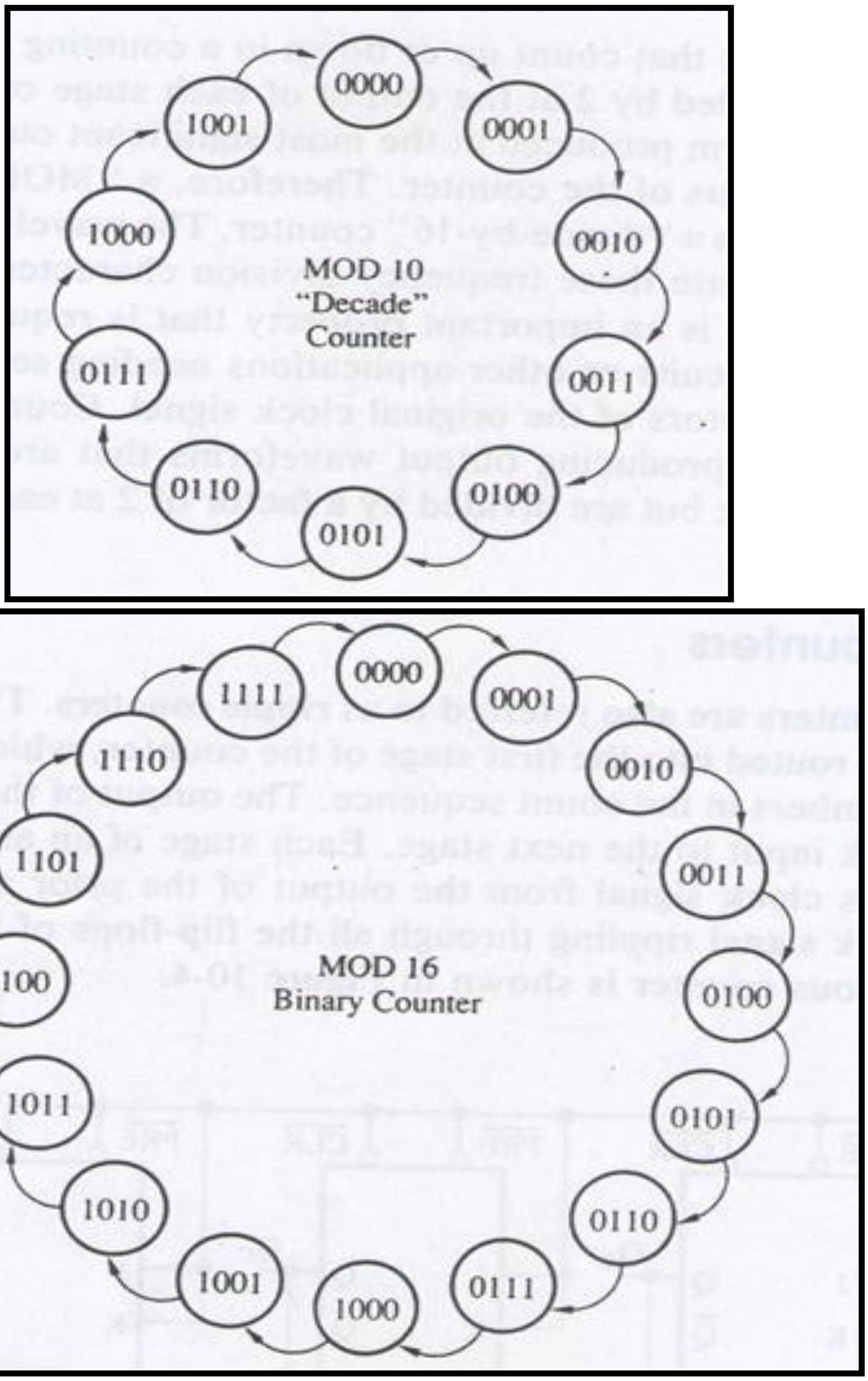

Figure (3): Counter State Transition Diagrams.

2. Counter Stages or Bits

The number of **output bits** of a counter is equal to the flip-flop stages of the counter. A MOD-2^n counter requires n stages or flip-flops in order to produce a count sequence of the desired length. The first stage of a counter is the **least significant bit (LSB)**. The last stage of a counter is the **most significant bit (MSB)**.

3. Frequency Division

Digital counters function as frequency dividers since they *divide the input control clock frequency by the modulus of the counter.* As shown in Example (2) for binary counters that count up or down in a counting sequence, the clock frequency is divided by 2 at the output of each stage of the counter.

The output waveform produced at the most significant output stage has a frequency of 1/modulus of the counter. Therefore, a "MOD-16" counter can also be referred to as a "divide-by-16" counter. The waveform in Figures (1 and 2) demonstrates these frequency division characteristics.

Frequency division is an important property that is required when designing digital clock circuits or other applications needing several frequencies that are integer factors of the original clock signal. Counters serve the significant function of producing output waveforms that are synchronous "with the incoming clock but are divided by a factor of 2 at each stage of the counter.

4. Asynchronous Counters

Asynchronous counters are also referred to as ripple counters. The incoming clock waveform is routed into the first stage of the counter, which generates the LSB of the numbers in the count sequence. The output of the LSB stage serves as the clock input to the next stage. Each stage of an asynchronous counter obtains its clock signal from the output of the prior stage, which results in the clock signal rippling through all the flip-flops of the counter. A 4-bit asynchronous counter is shown in Figure (4).

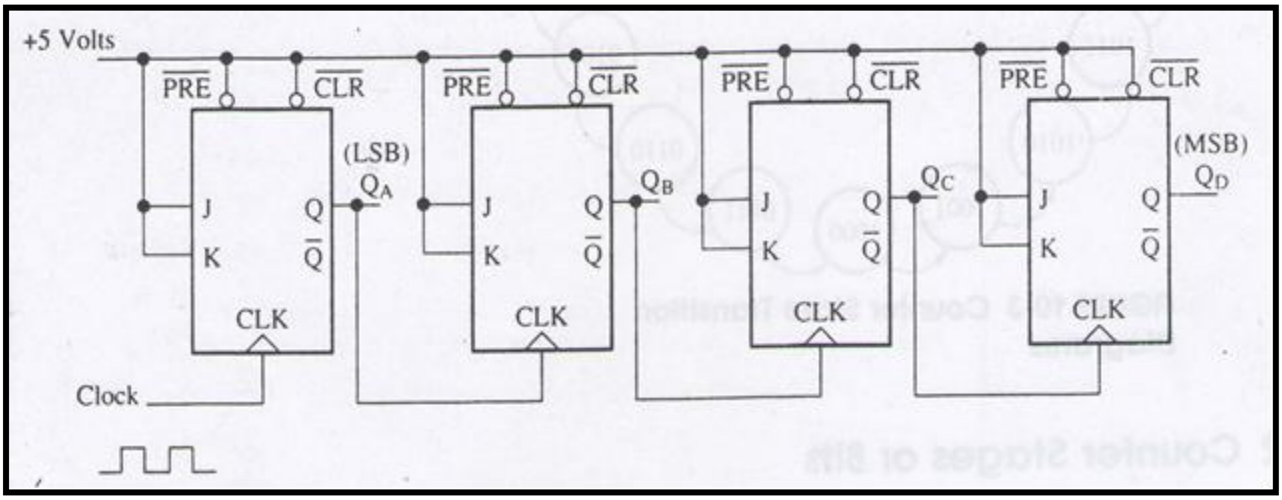

Figure (4): Four-Bit Asynchronous Counter.

5. Synchronous Counters

Synchronous counters are constructed with one common clock signal as the input to all the flip-flops simultaneously. The clock does not ripple through the counter stages. Synchronous counters are also referred to as parallel counters due to the parallel manner that the clock is fed to all the counter stages. Figure (5) shows the basic configuration of a 4-bit synchronous counter.

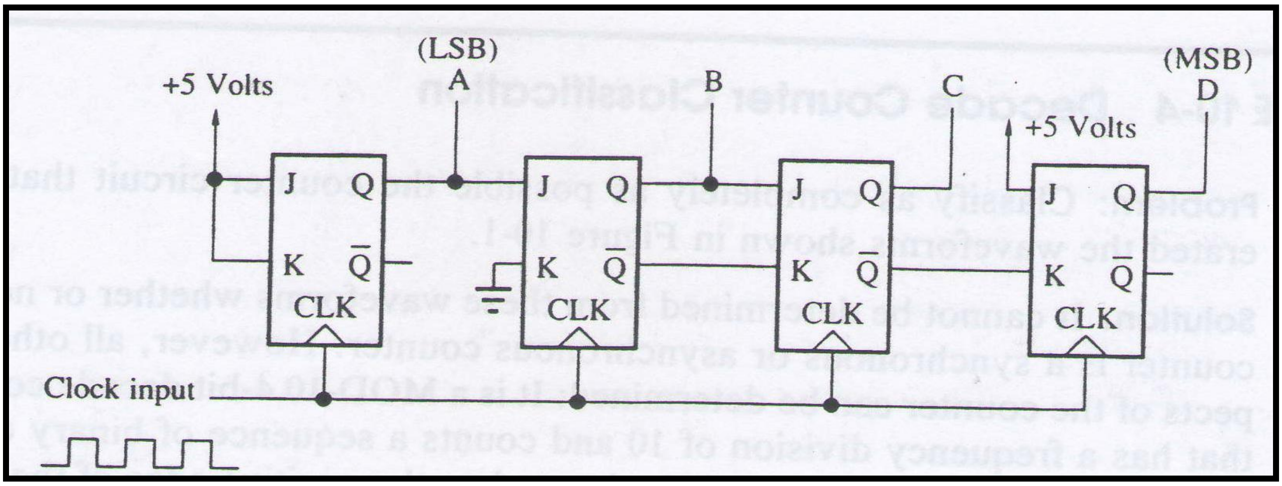

Figure (5): Four-Bit Synchronous Counter.

6. Counter Triggering

A counter is classified as a **positive edge-triggered** or **negative edge-triggered** device, depending on the trigger characteristic of the flip-flop circuits that form the counter. It is important to know the triggering of the counter because the count states only change on the triggering edge of the incoming clock. Figure (6) compares the output waveforms for a positive edge-triggered and negative edge-triggered 4-bit binary counter. Notice the timing shift relative to the incoming clock pulse.

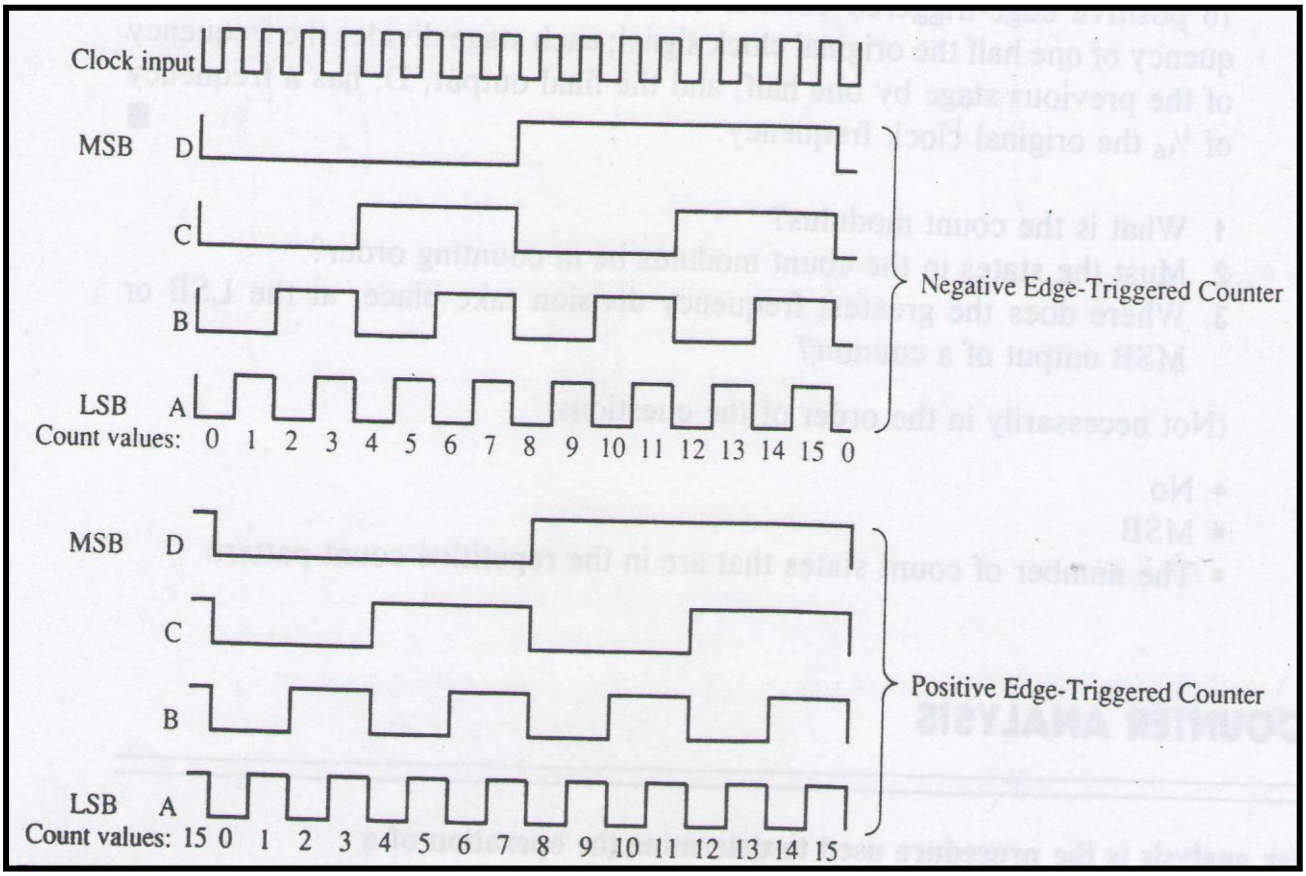

Figure (6): Negative Edge-Triggered versus Positive Edge-Triggered Counter Waveforms.

EXAMPLE (4): Decade Counter Classification

Problem: Classify as completely as possible the counter circuit that generated the waveforms shown in Figure (1).

***Solution*:** It cannot be determined from these waveforms whether or not the counter is a synchronous or asynchronous counter. However, all other aspects of the counter can be determined: It is a MOD-10 4-bit decade counter that has a frequency division of 10 and counts a sequence of binary coded decimal (BCD) values from 0 to 9 triggered on the positive edge of the input clock.

***EXAMPLE (5):* Binary Counter Classification**

Problem: Classify the 4-bit binary counter circuit that generated the waveforms in Figure (2).

Solution: As stated in Example (3), the waveforms shown cannot positively identify the counter circuit as synchronous or asynchronous. However, all other characteristics can be classified. The binary counter is a 4-bit MOD-16 positive edge-triggered counter circuit. The **A** output stage has a frequency of one half the original clock signal; each stage divides the frequency of the previous stage by one half; and the final output, **D**, has a frequency of (1/16) the original clock frequency.

Section Self-Test

1. What is the count modulus?
2. Must the states in the count modulus be in counting order?
3. Where does the greatest frequency division take place, at the LSB or MSB output of a counter? (Not necessarily in the order of the questions)

ANSWERS: (Not necessarily in the order of the questions).

- No.
- MSB.
- The number of count states that are in the repetitive count pattern.

COUNTER ANALYSIS

Counter analysis is the procedure used to determine the operation of a counter circuit and to classify the operation. The counter circuit must be analyzed to determine the modulus, the "divide-by" factor of the counter, the number of stages, whether it is asynchronous or synchronous, the triggering of the flip-flops, whether it is an up or down counter, and the count sequence of the counter.

A counter circuit should be analyzed following these seven steps:

1. *Observe the counter system clock.* If it is common to all flip-flop stages, the counter is synchronous. If it is not common to all flip-flop stages, the counter is **asynchronous.**

2. *Determine the number of stages of the counter by counting the flip-flops or outputs.*
3. *Observe the type of flip-flops used in the counter circuit, noting their triggering and operation. Most asynchronous counters are built from toggle flip-flops.*
4. *For asynchronous counters built with toggle flip-flops, determine the operation of the counter through waveform analysis.*
5. *Determine the output waveforms from the clock stages relative to the input clock waveform. For toggle flip-flops, the output signal changes from HIGH to LOW continuously on the clock trigger point.*
6. *Determine the modulus of the counter.*
7. *Construct a state transition diagram to describe the counter operation.*

***EXAMPLE (6):* Two-Bit Binary Counter Analysis**

Problem: Analyze the 2-bit counter shown in Figure (7).

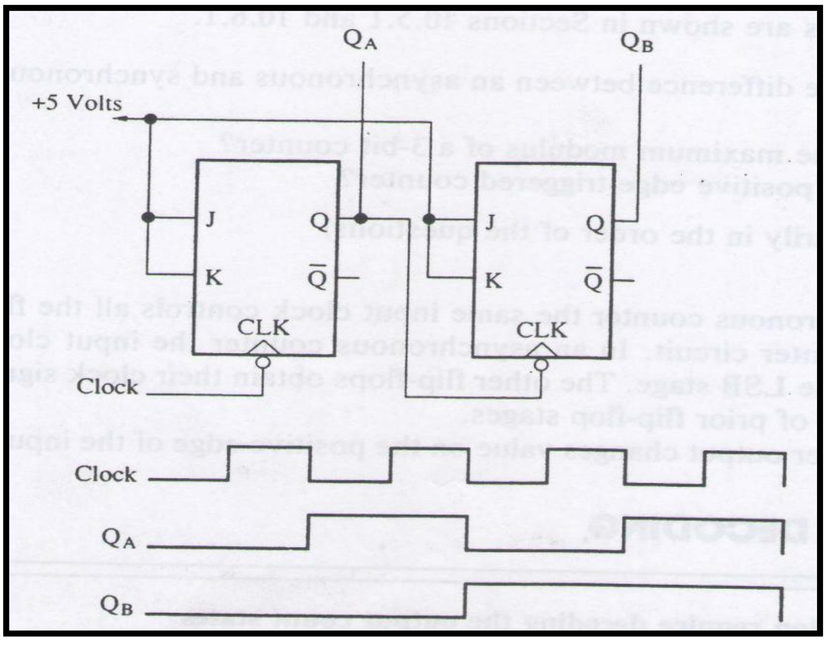

Figure (7): Two-Bit Binary Counter Analysis.

Solution: The counter in Figure (7) has two flip-flops and two output bits; therefore it is a two stage counter. The input clock does not trigger both flip-flops, and thus it is an asynchronous counter circuit. The Q_A output is used as the clock to the second stage of the flip-flop. The J-K flip-flops have the J and K inputs tied high, so they are considered toggle flip-flops. The flip-flops are shown as negative edge-triggered devices. The waveforms are analyzed to determine the count sequence. The initial state of Q_A and Q_B is assumed to be a logic LOW. The waveforms are drawn so that the Q_A output triggers on the negative edge of the input clock and the Q_B output triggers on the negative edge of the Q_A output.

From the waveforms it can be seen that Q_A is the LSB of the count sequence, and its frequency is one half the input clock frequency. The Q_B output is the MSB of the count sequence, and its frequency is one quarter the input clock frequency. The count sequence can be determined from the waveform. The sequence is listed here.

Q_B	Q_A
0	0
0	1
1	0
1	1

From the count sequence it is determined that the counter is a MOD-4 binary up counter.

More complex examples of the analysis of synchronous and asynchronous counters are shown in the next sections.

Section Self-Test

1. What is the difference between an asynchronous and synchronous counter?
2. What is the maximum modulus of a 3-bit counter?
3. What is a positive edge-triggered counter?

ANSWERS: (Not necessarily in the order of the questions).

- 8.
- In a synchronous counter the same input clock controls all the flip-flops in the counter circuit. In an asynchronous counter the input clock only controls the

LSB stage. The other flip-flops obtain their clock signal from the output of prior flip-flop stages.

- The counter output changes value on the positive edge of the input clock.

COUNT STATE DECODING

Counter applications often require decoding the output count states produced by a counter. Counter decoding can be used to shorten sequence, to enable other logic circuits when a specific count state is reached, or to display the count state as a decimal number.

Decoding a count state means that a signal is activated for only one count state. Simple active HIGH decoding can be accomplished with an AND gate, whereas active-LOW decoding requires the use of a NAND gate.

Count states are decoded by forming a "min-term" of the variables that represent the desired count sequence. For example, in order to decode the output state 1101, the output variables $Q_D Q_C Q'_B Q_A$ are ANDed together. The output from the AND gate is high only when the input logic levels represent the value 13. Replacing the AND gate with a NAND gate would result in an active-LOW output signal for the decoded count state of 1101.

If numerous count states have to be decoded, then a digital IC decoder such as the 74LS138 or 74LS154 should be used to simplify the circuitry. When the count states have to be decoded and displayed, a display decoder/driver such as the 74LS47 can be used with a light emitted diode (LED) display.

EXAMPLE (7): Counter State Decoding

Problem: In the case of the binary counter that generated the waveforms shown in Figure (2), determine the terms required for active-LOW decoding of states 1, 3, 9, 12, and 15.

Solution: The output values of the states to be decoded are listed here along with the min-term required for active-LOW decoding of each state:

Count State	D	C	B	A	Decoding Min-term			
1	0	0	0	1	D'	C'	B'	A
3	0	0	1	1	D'	C'	B	A
9	1	0	0	1	D	C'	B'	A
12	1	1	0	0	D	C	B'	A'
15	1	1	1	1	D	C	B	A

Section Self-Test

1. What is meant by "decoding" a count state?

2. When should NAND gates be used for count state decoding'?

3. When should an IC decoder, such as the 74138 or 74154 be used for count state decoding?

ANSWERS: (Not necessarily in the order of the questions).

- For active-LOW decoding
- When several count states must be decoded, an IC decoder can decode numerous count states with a single IC. Individual logic gates, such as NANDs or ANDs, require one gate and inverters for each decoded state, resulting in the use of several ICs.
- The occurrence of a single count state activates a logic circuit to produce an output signal.