ASYNCHRONOUS COUNTER CIRCUITS

Asynchronous counters do not have a common clock that controls all the Hip-flop stages. The control clock is input into the first stage, or the LSB stage of the counter. The clock for each subsequent stage is obtained from the output from the prior flip-flop stage.

Toggle flip-flops are used almost exclusively in the design of asynchronous counters. With the toggle flip-flop, the output state toggles between a logic HIGH and a logic LOW on each clock pulse. The external clock that controls the flip-flop output state is input into the LSB stage. Either the true or inverted output from the flip-flop can serve as the output bit value to form the count state or as the clock to the next stage in the counter circuit.

For any given asynchronous counter circuit, the count direction for counting serially up or down is dependent on the triggering of the flip-flops. An asynchronous counter designed for positive edge-triggered flip-flops will not generate the desired count sequence if negative edge-triggered flip-flops are substituted in the circuit design. Analyzing waveforms into and out of the flip-flops is crucial to obtaining a properly functioning circuit.

Asynchronous counters often experience many timing and glitch problems due to the cumulative propagation delays resulting from the clock ripple action through the flip-flop stages. The effects of the delays worsen with increased counter size and limit the input clock rate.

The design procedures for asynchronous serial counters are relatively simple. Techniques for analyzing the operation and designing asynchronous counters are the subject of the next sections.

Asynchronous Counter Analysis

Asynchronous counter analysis is carried out according to the procedures specified in above. A detailed procedure to follow for analyzing asynchronous counters is demonstrated in Examples (8 and 9).

EXAMPLE (8): Asynchronous Counter Analysis

Problem: Analyze the operation of the counter in Figure (4).

Solution: By observing the circuit in Figure (4), it can be seen that it is a 4-bit positive edge-triggered asynchronous counter.

Begin the waveform analysis by drawing an input clock waveform Assume a 50% duty cycle unless otherwise known. Then graph the output waveforms from each flip-flop stage of the counter. Note that only the *LSB* stage is triggered by the input clock; all other stages are triggered by an output from the previous stage. The waveforms are shown in Figure (8).

The state transition diagram, derived from the waveforms, is shown in Figure (9).

The counter classification is completed by summarizing the characteristics displayed in the state transition diagram:

- MOD 16.
- Divide by 16.

- Asynchronous.
- Four-bit.
- Positive edge-triggered.
- Binary down counter.

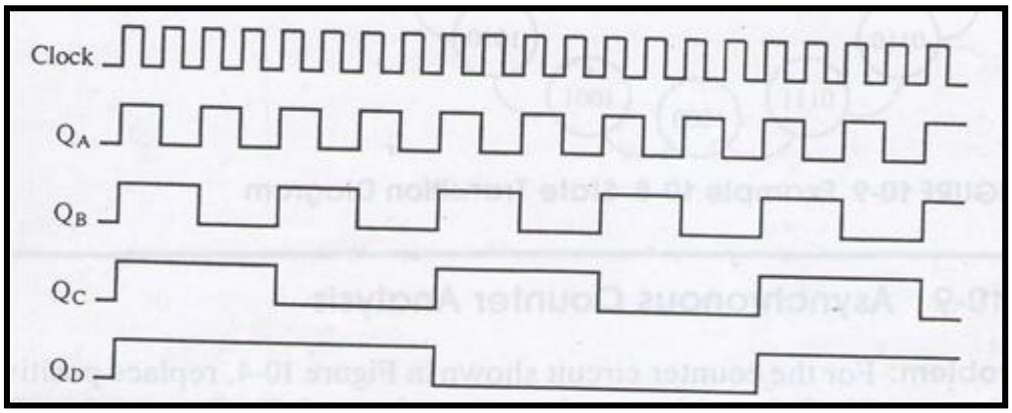

Figure (8): Example (8) Waveforms.

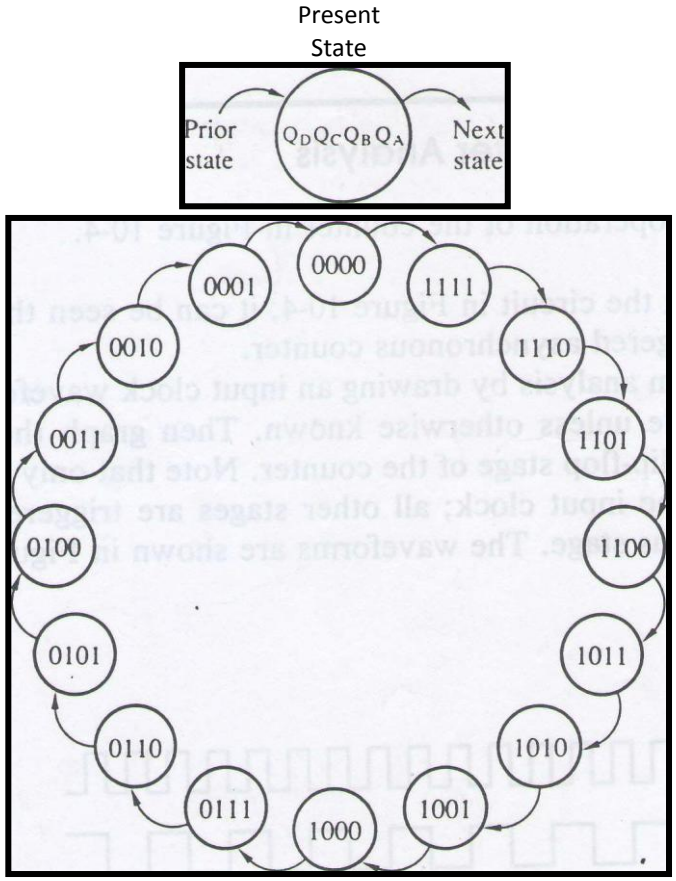

Figure (9): Example (8) State Transition Diagram.

EXAMPLE (9): Asynchronous Counter Analysis

Problem: For the counter circuit shown in Figure (4), replace positive edge-triggered flip-flops with negative edge-triggered flip-flops and analyze the operation of the circuit.

Solution: The output waveforms are graphed in Figure (10) to determine the operation of the counter.

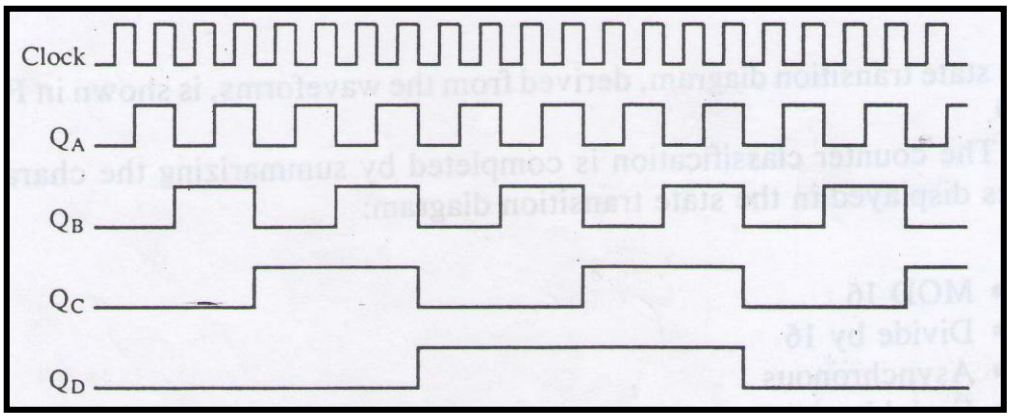

Figure (10): Example (9) Waveforms.

By observing the output waveforms, it can be seen that the count direction has changed just by changing the triggering characteristic of the flip-flop forming the counter. The state transition diagram for this circuit is shown in Figure (11).

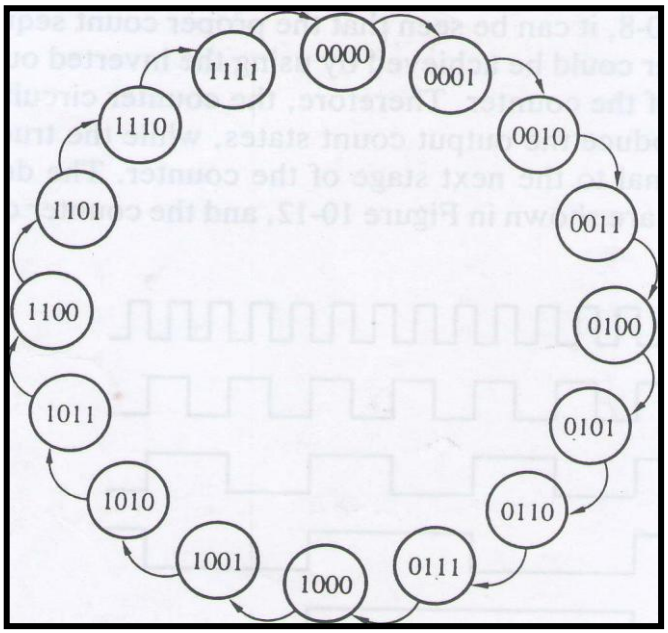

Figure (11): Example (9) State Transition Diagram.

The counter classification is summarized here:

- MOD 16.
- Divide by 16.
- Asynchronous.
- Four-bit.
- Negative edge-triggered.
- Binary up counter.

Asynchronous Counter Design

Asynchronous counters that count in a serial count sequence of up or down can be designed by matching flip-flop circuit performance to the output wave form requirements. These procedures should be followed:

1. *Specify the operational requirements of the counter,* including the number of *stages, modulus,* and *trigger characteristics.*
2. *Graph the required output waveforms.*
3. *Determine the necessary output to use as the clock input to the following stage.* Either the true or complemented output could serve as the clock signal.
4. *Verify the design through analysis and testing.*

EXAMPLE (10): Asynchronous Counter Design

Problem: Design a 4-bit, MOD-16, asynchronous binary up counter using positive edge-triggered toggle flip-flops.

Solution: By observing the output waveforms for a binary up counter, such as those shown in Figure (8), it can be seen that the proper count sequence for a 4-bit binary up counter could be achieved by using the inverted outputs from the flip-flops stages of the counter. Therefore, the counter circuit uses the inverted outputs to produce the output count states, while the true outputs provide the clock signal to the next stage of the counter. The desired counter output waveforms are shown in Figure (12), and the counter circuit is shown in Figure (13).

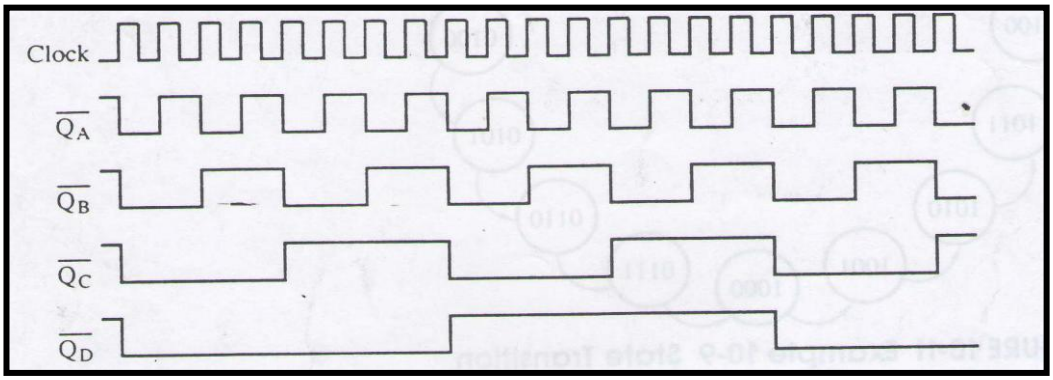

Figure (12): Example (10) Waveforms.

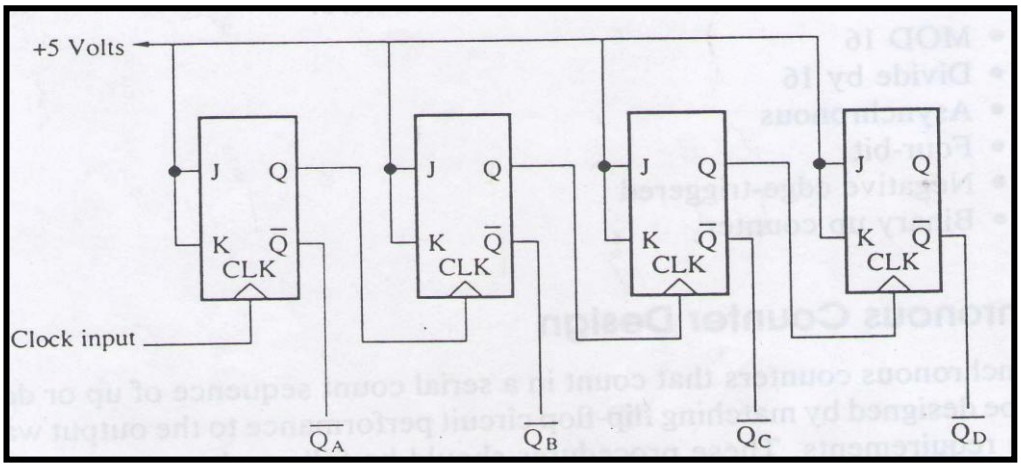

Figure (13): Example (10) Asynchronous 4-Bit Binary Up Counter.

EXAMPLE (11): Counter Decoding

Problem: Design a MOD-10 asynchronous counter by shortening the count sequence of the counter circuit designed in Example (10). *(Hint:* Use the active-LOW asynchronous clear input on the flip-flops to reset the counter to zero).

Solution: A decade or MOD-10 counter can be designed that counts only from 0 to 9. The MOD-16 counter of Example (10) can be redesigned to produce a MOD-10 count sequence by adding a decoding circuit. The decoding circuit resets the counter back to zero after the ten count states so that it only counts 0 to 9 repetitively.

The counter will produce the output 1 0 1 0 as its eleventh count state, but this state is not desired. Therefore, decode the output state 1 0 1 0 and reset the counter back to zero using the asynchronous clear inputs to the flip-flops. Decoding the state 1 0 1 0 and clearing the counter to 0 0 0 0 results in a glitch in one of the waveforms. This glitch serves as the clear signal to reset the flip-flops. Figure (14) shows the modified counter circuit and Figure (15) shows the resulting output waveforms.

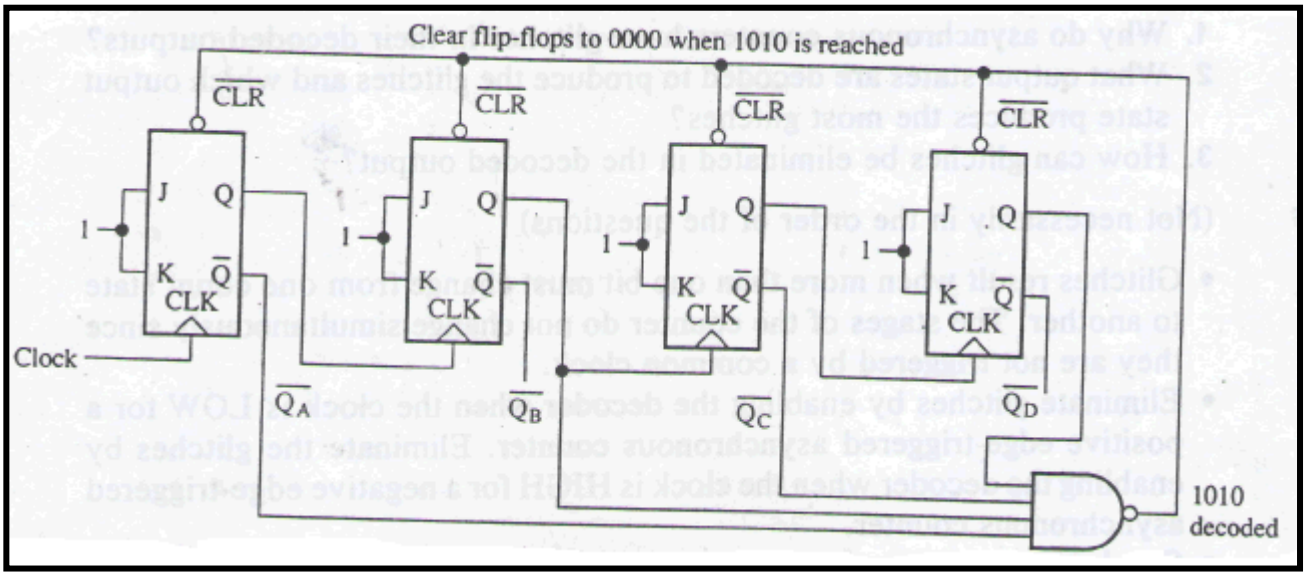

Figure (14): Example (11) Asynchronous Decade Counter Circuit.

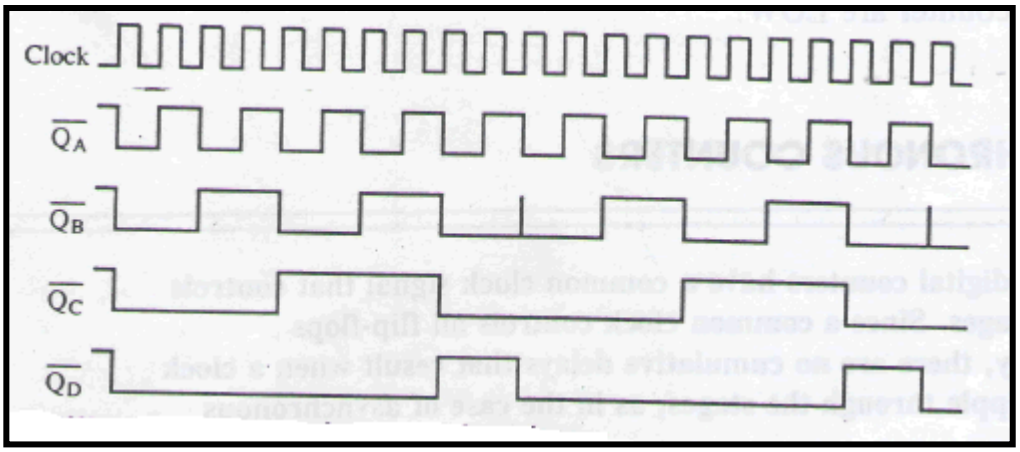

Figure (15): Example (11) Waveforms.