

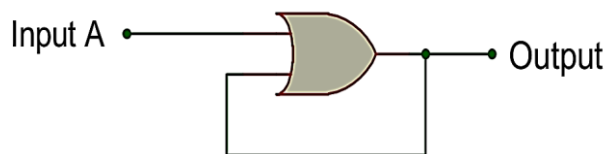
Chapter Seven

7.1 Introduction:

The sequential logic studies digital circuits which functions in such a way that their outputs logic states depend not only on the logical combination of their inputs states, but also on the memory of the circuit. In fact, at a given instant, sequential circuits always store the status of their output and that status cannot change unless new logic signals are sent to its inputs: this is the memory effect. The simplest sequential logic circuit is the latch which is a circuit capable of storing one bit of information. It has two outputs, one being the reverse of the other. A flip-flop is an edge triggered latch; it means that it cannot function unless the right signal edge (either rising or falling edge) is available at its clock input. This chapter is an introduction to sequential logic; it is focused on the study of latches and flip-flops which are tools used in the designing of sequential circuits.

7.2 Multivibrators:

Let us consider the following circuit:



According to the functioning of the OR gate, if $A = 1$, the output must be 1. However, if A is in low logic state, we cannot guarantee the logic state of the output.

Since the output feeds back to one of the OR gate inputs, this circuit will “latch” (That is to remain unchanged) in the 1 output state after any time that A is 1.

In fact, when $A = 0$, the output could be 0 or 1 depending on the circuit previous state. So the output maintains (or memorises) its last state when A is 0. The truth table of our circuit can be given as follow.

Input A	Output
0	latch
1	1

Any circuit employing feedback is called multivibrator. A bistable multivibrator can hold stable in one of two possible states (either 0 or 1). Monostable multivibrator

holds stable only in one output state, the other state being momentary. Astable multivibrator has no stable state. It oscillates back and forth between an output of 0 and 1. One of the most common multivibrators is the integrated circuit NE555, which can work as well as monostable or astable.

7.2.1 Latches:

Many latches exist, but their common characteristic is that they can store one bit of information.

7.2.1.1 The S-R latch:

The S-R latch is a bistable multivibrator having two stable states: Set and Reset. So S-R latch means Set-Reset latch. To create an S-R latch, can wire two NOR gates in such a way that the output of one feeds back the input of another, and vice versa.

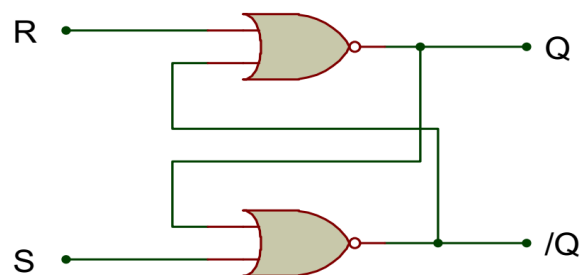


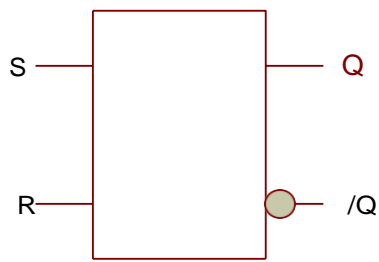
Figure 7.1: Principle diagram of an S-R latch.

- Truth table:

S	R	Q	/Q
0	0	Latch	
0	1	0	1
1	0	1	0
1	1	invalid	

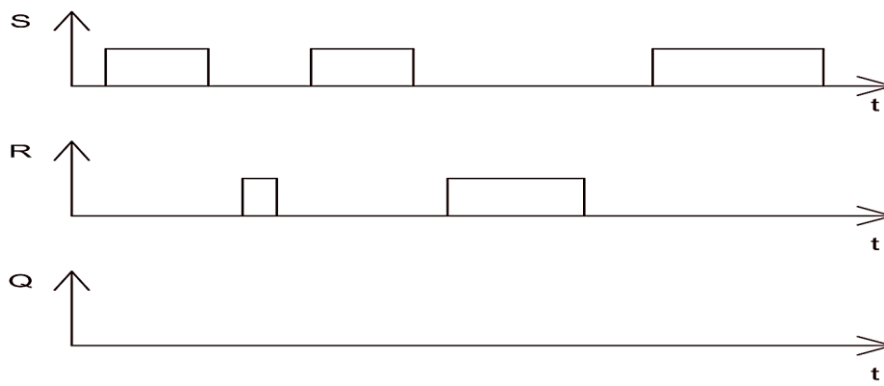
- The outputs Q and /Q should always be in opposite logic states.
- Making both S and R inputs equal to 1 results in both Q and /Q being 0: this is why this inputs combination is forbidden, it produces an invalid or illegal state.
- Making S = 1 and R = 0 sets the multivibrator so that Q = 1 and /Q = 0.
- Making R = 1 and S = 0 resets the multivibrator so that /Q = 1 and Q = 0.
- When R = 0 and S = 0 the multivibrator outputs latch in their previous states.

- Circuit diagram:

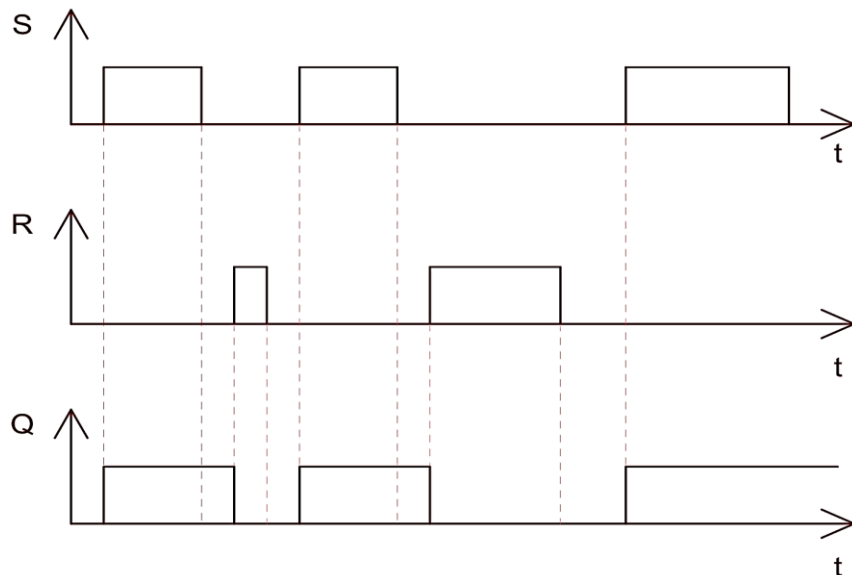


Exercise 7.1:

The following waveforms are applied at the inputs of an S-R latch. Deduce the waveform of the output assuming that the initial state of the output is $Q = 0$.



The waveforms of the output Q of the exercise above can be given as follows:



7.2.1.2 The gated S-R latch:

The gated S-R latch has an enable input E which must be activated in order to allow the latch to take into consideration the combinations available at its inputs. The latch would not function properly unless the right logic level is sent to the input E . the principle diagram of a gated S-R latch is given bellow.

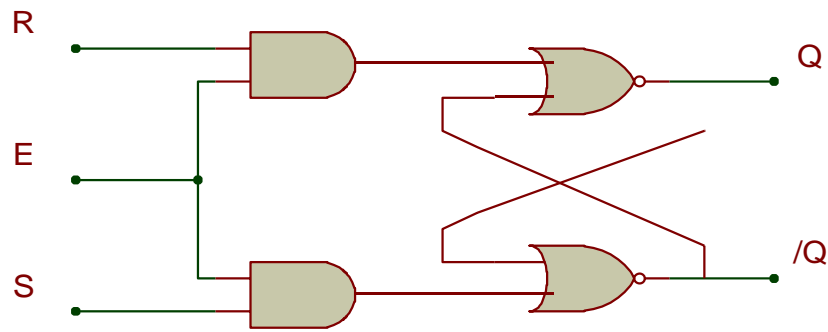


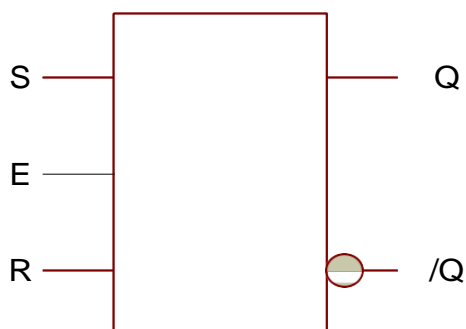
Figure 7.2: Principle diagram of a gated S-R latch.

- Truth table:

E	S	R	Q	/Q
0	X	X	Latch	
1	0	0	Latch	
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	

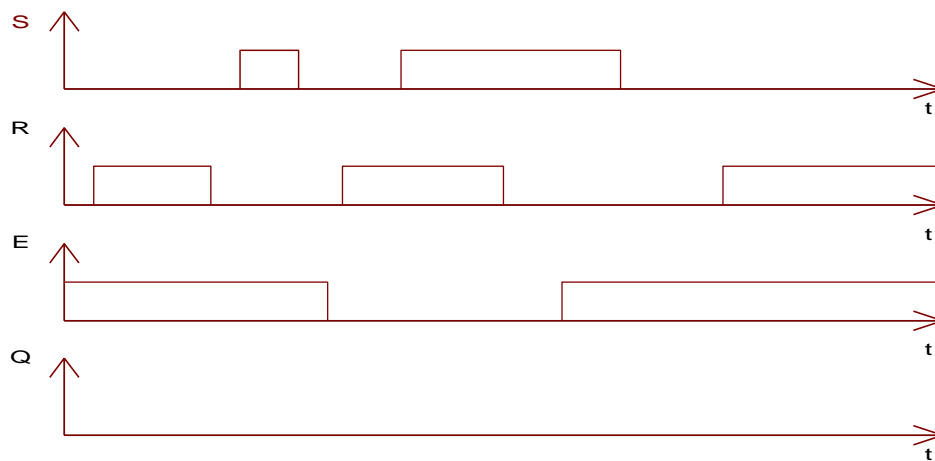
When $E = 0$, the outputs of the two AND gates are forced to 0, regardless of the states of either S or R. The previous states of the outputs are therefore memorised. Only when the enable input is activated (by sending a 1 to it) will the latch respond to the S and R inputs.

- Circuit diagram:

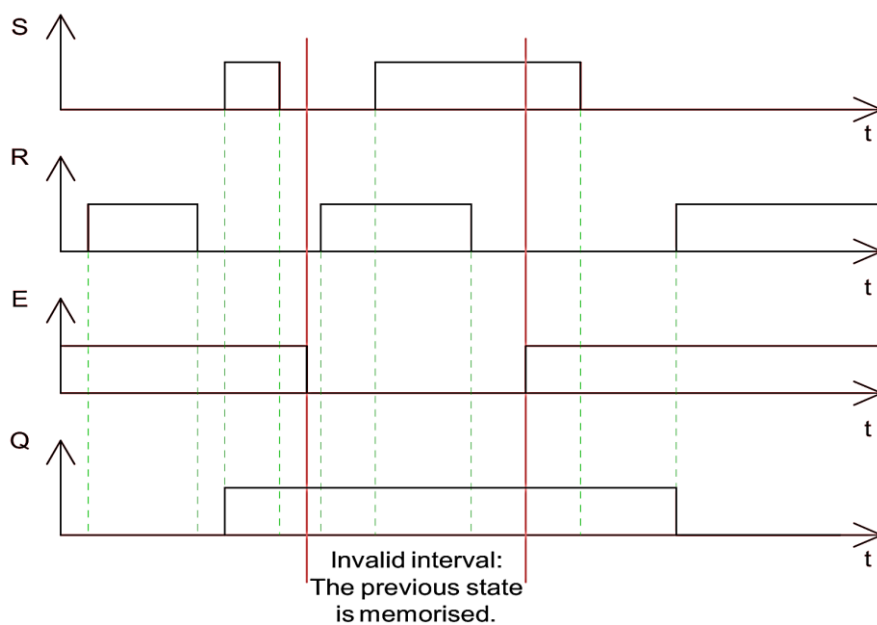


Exercise 7.2:

The following waveforms are applied at the inputs of a gated S-R latch. Deduce the waveform of the output assuming that the initial state of the output is $Q = 0$.



The waveform of the output Q of the exercise 7.2 above can be given as follows:



7.2.1.3 The D latch:

The D latch has no illegal input state because the inputs S and R are always in opposite state. The principle diagram of a D latch is given bellow:

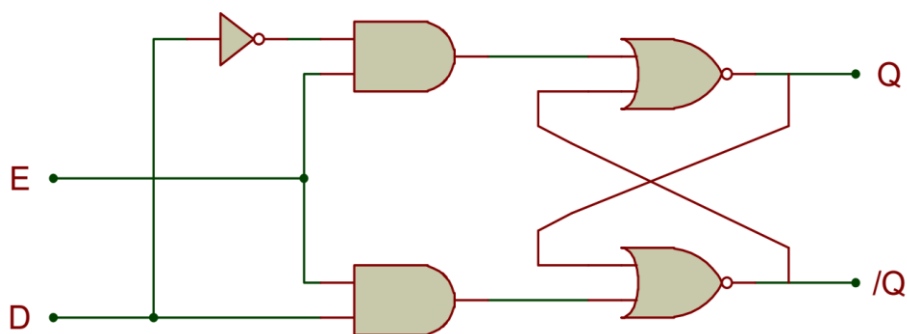


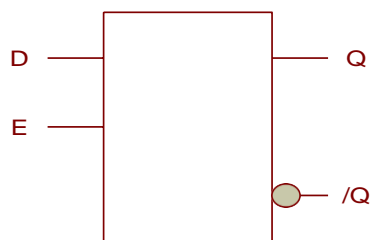
Figure 7.3: Principle diagram of a D latch.

- Truth table:

E	D	Q	/Q
0	X	Latch	
1	0	0	1
1	1	1	0

When the enable input is high, the output Q copies the state available at the input. When E = 0, the circuit remain latched in its previous state.

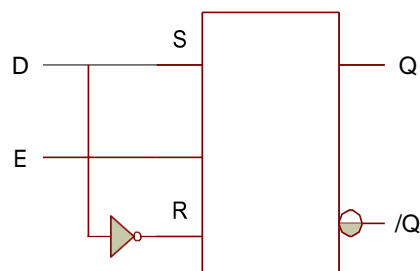
- Circuit Diagram:



An application for D latch is a 1 bit memory circuit. You can store a 0 or 1 bit in a D latch by making the enable input high and setting the input D to whatever you want the stored bit to be.

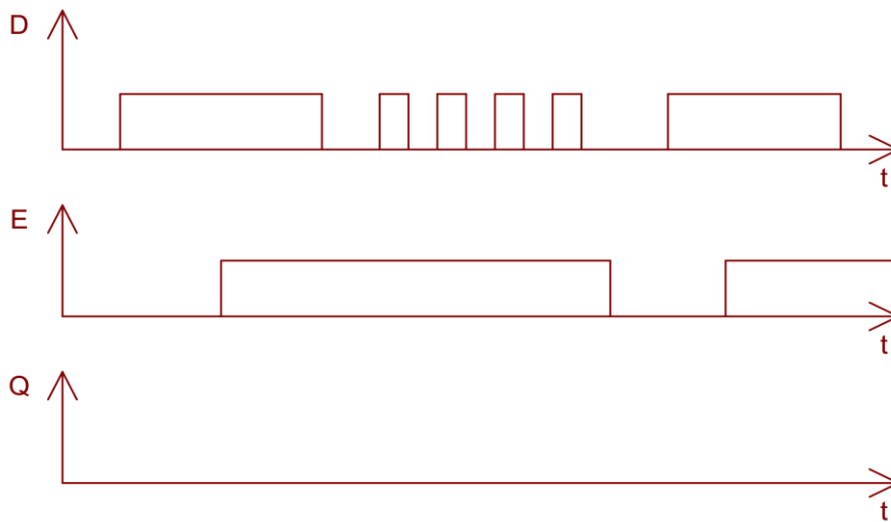
Remark 7.1: Designing a D latch using an S-R latch.

The D latch is nothing more than a gated S-R latch with an inverter added to make the complement of S, as shown in the following diagram.

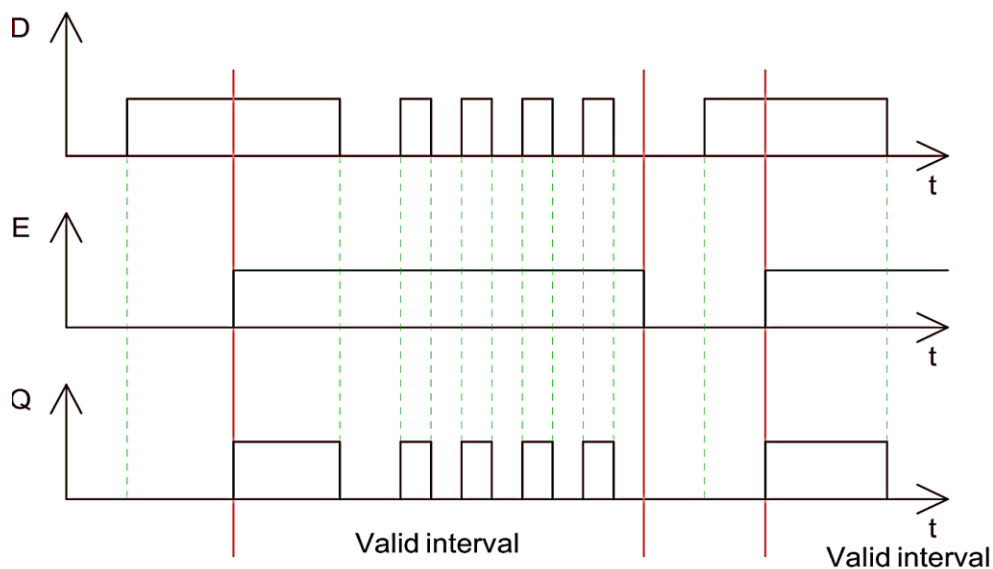


Exercise 7.3:

The following waveforms are applied at the inputs of a D latch. Deduce the waveform of the output assuming that the initial state of the output is Q = 0.



The waveform of the output Q of the exercise 7.3 above can be given as follows.



We can notice that within the valid interval, the output of the D latch just copies the waveform of the input. When the enable input is made low, the latch ignores the status of the D input and merrily holds the stored bit value.

7.2.2 The edge triggered latches: Flip-flops

We have studied both S-R and D latch circuits with an enabling input. The latch responds to input's data only when the enabling input E is activated. In many digital applications however, it is desirable to limit the responsiveness of a latch circuit to a very short period of time instead of the entire duration that the enabling input is activated. Another method of enabling a multivibrator circuit is called edge triggering. For this method, the circuit's data inputs have control only during the time during which the enabling input is transitioning from one state to another. There are two types of edge triggering:

- If the enabling input functions when transitioning from low state to high state (from 0 to 1), the latch is said to be positive edge triggered.
- If the enabling input functions when transitioning from high state to low state, the latch is said to be negative edge triggered.



Any latch whose enable input is edge triggered is a flip-flop. So we can say that a flip flop is an edge triggered latch. An S-R flip-flop is an edge triggered S-R latch and a D flip-flop is an edge triggered D latch.

7.2.2.1 Edge triggered D latch: D flip-flop:

Let us study a positive edge triggered D latch. It responds to the D input only during the brief instant when the enabling signal transitions from low to high. The principle diagram of D flip-flop is given as follows.

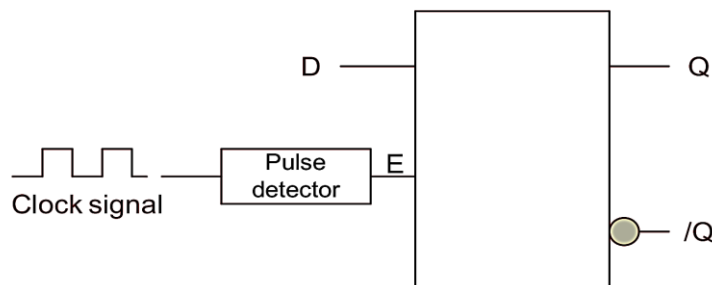
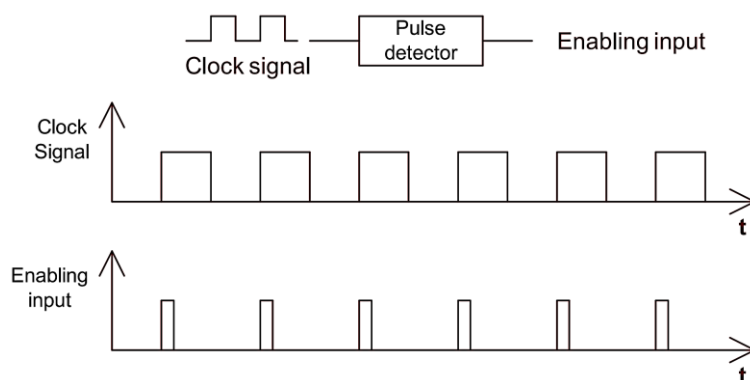


Figure 7.4: Principle diagram of a D flip-flop.




Remark 7.2: The pulse detector

A pulse detector is connected to the enable input of the latch. It is a circuit that outputs a brief pulse when the right transition of the clock signal occurs (either rising or falling transition).



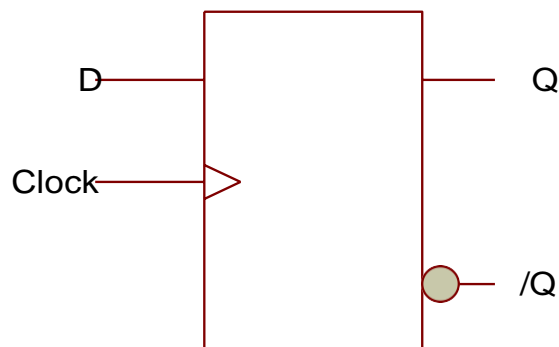
The pulse detector enables the latch for a brief moment; after the pulse, the latch holds its output at the same state till another pulse occurs.

- Truth table:

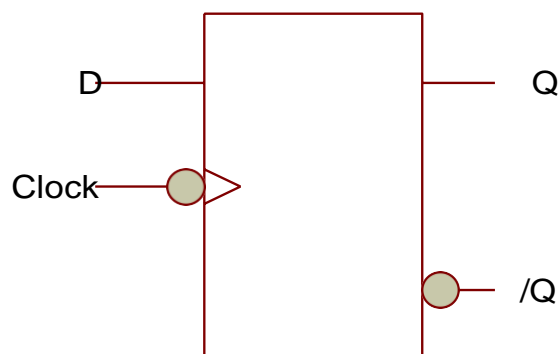
Clock	D	Q	/Q
	X	Latch	
	0	0	1
	1	1	0

The input D will have no effect unless the clock signal is transitioning from low to high. Otherwise, the flip-flop's outputs latch in their previous states.

- Circuit diagram:

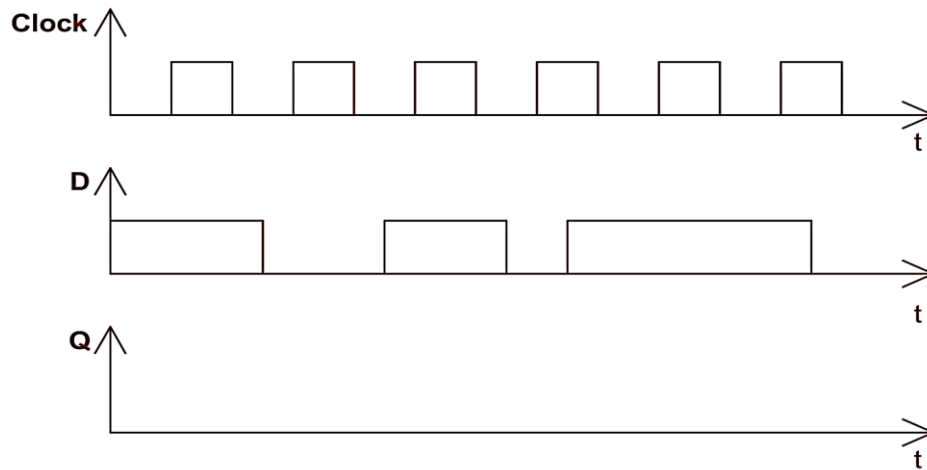


If we had a negative edge triggered D flip-flop, the circuit diagram would have been as follows.

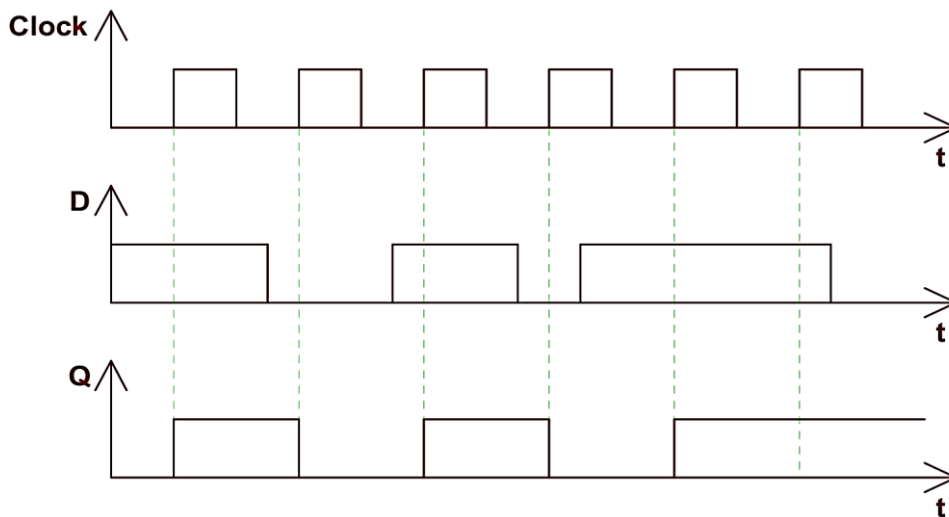


Exercise 7.4:

The following waveform is applied at the inputs of a positive edge triggered D flip- flop. Determine the waveform of the output Q assuming that it is initially at low logic state.



The waveform of the output Q of the exercise 7.4 above can be given as follows.



7.2.2.2 S-R Flip-flop:

An S-R flip flop is an edge triggered S-R latch. A pulse detector is connected to its enable input in order to detect rising or falling edges of the clock signal. The principle diagram is as follows.

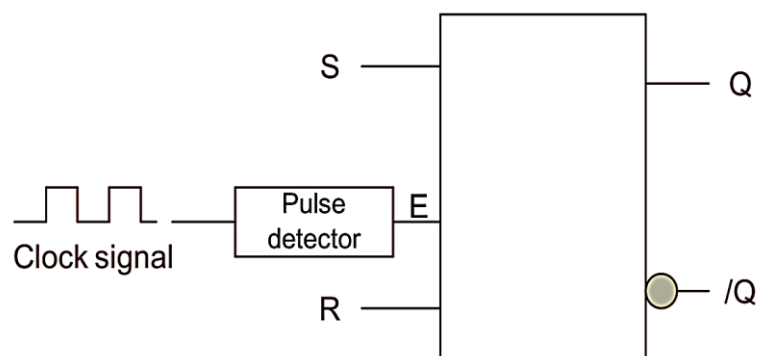


Figure 7.5: Principle diagram of an S-R flip-flop.

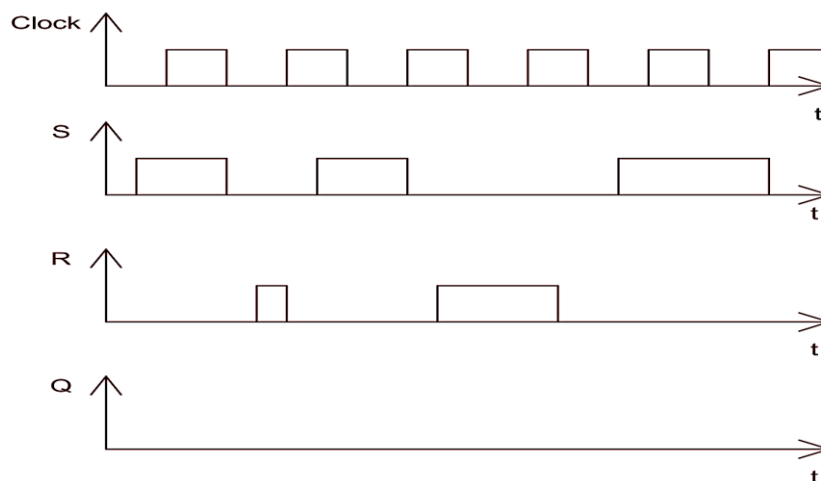
- Truth table:

Clock	S	R	Q	/Q
	X	X	Latch	
	0	0	Latch	
	0	1	0	1
	1	0	1	0
	1	1	Invalid	

Only when the clock signal is transitioning from low to high is the circuit responsive to the S and R inputs. For any other condition of the clock signal, the circuit will be latched.

Exercise 7.5:

The following waveforms are applied at the inputs of an S-R flip-flop. Determine that of the output Q assuming that it is initially at low logic state.



7.2.2.3 The J-K flip-flop:

The J-K flip flop is a modified version of an S-R flip-flop with no invalid output state. When $J = 1$ and $K = 1$, and the clock input is pulsed, instead of an invalid state at the output, the circuit will toggle to a state opposite of that was previously available at its output: if the output was previously 1, it toggles to 0 and vice versa. The principle diagram of a J-K flip-flop is given as follows.

What used to be S and R inputs are now J and K inputs respectively. The previous two inputs AND gates have been replaced by three inputs AND gates. The third input of each gate receives feedback from Q and /Q outputs.

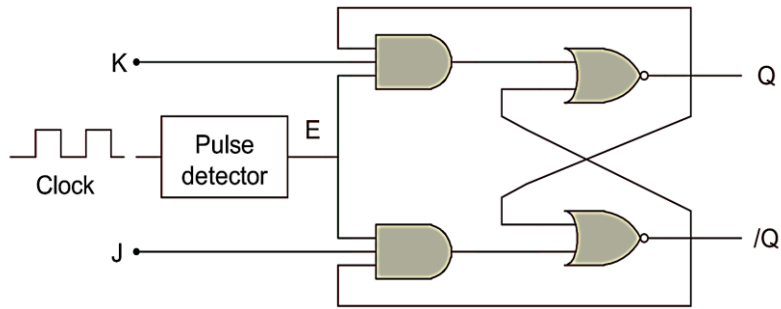
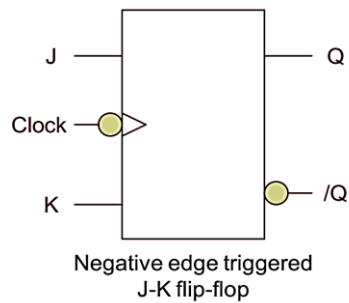
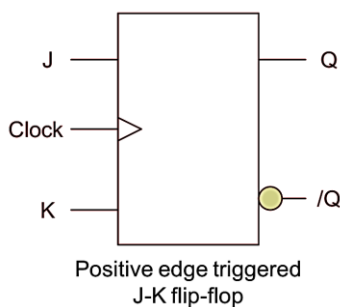


Figure 7.6: Principle diagram of a J-K flip-flop.

- Truth table:

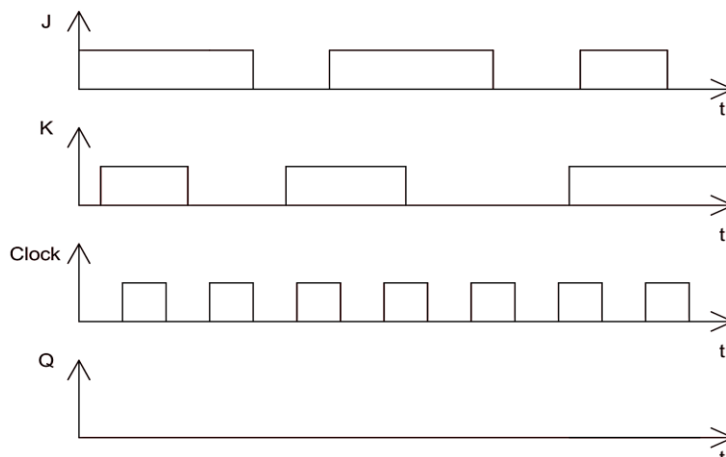
Clock	J	K	Q	/Q
	X	X	Latch	
	0	0	Latch	
	0	1	0	1
	1	0	1	0
	1	1	Toggle	

- Circuit diagram:

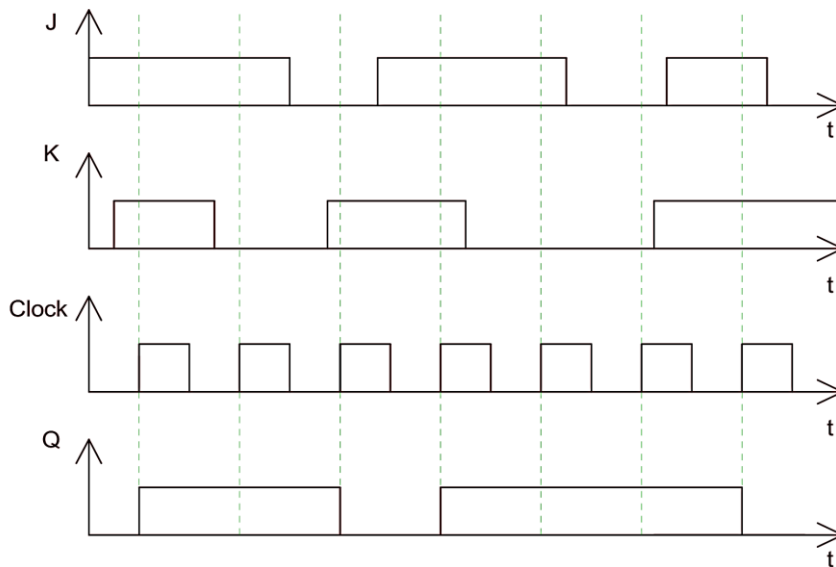


Exercise 7.6:

The following waveforms are applied at the inputs of a positive edge triggered J-K flip-flop. Determine that of the output Q assuming that it is initially at low logic state.

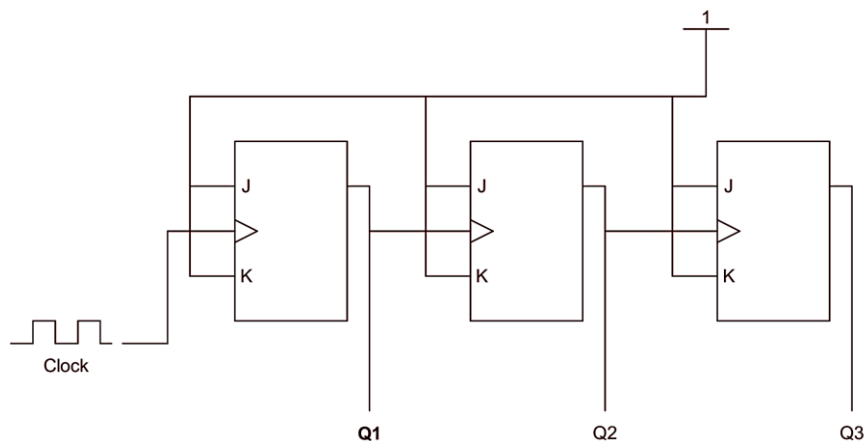


The waveform of the output Q of the exercise 7.6 above can be given as follows:



Exercise 7.7:

Let us consider the following digital system:



1. Draw the waveforms of the outputs Q1, Q2 and Q3.
2. Express the frequency f_1 , f_2 and f_3 of the waveforms of the outputs Q1, Q2 and Q3 respectively, in function of the frequency f_c of the clock signal.
3. Using the principle of the circuit above, design a digital system capable of dividing the frequency of the clock signal by 32.

7.2.3 Asynchronous flip-flop's inputs:

The normal data inputs to a flip-flop (D, S and R or J and K) are referred to as synchronous inputs because they have effect on the outputs (Q and \bar{Q}) only in synchronism with the clock signal transitions. Asynchronous inputs are some types of extra inputs which can set or reset the flip-flop regardless of the status of the clock signal. Typically, they are called PRESET and CLEAR.

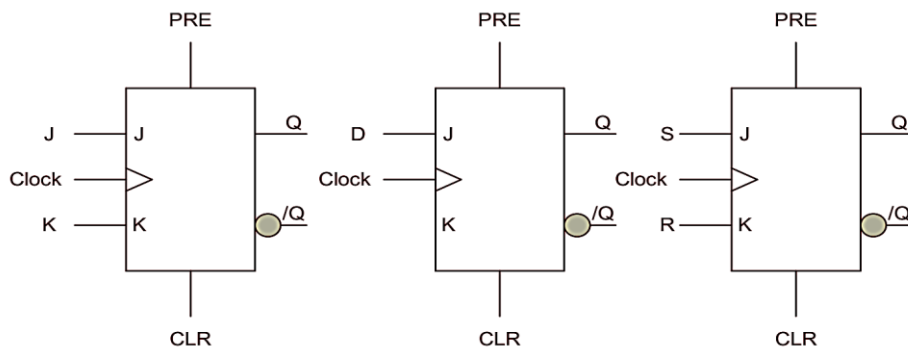
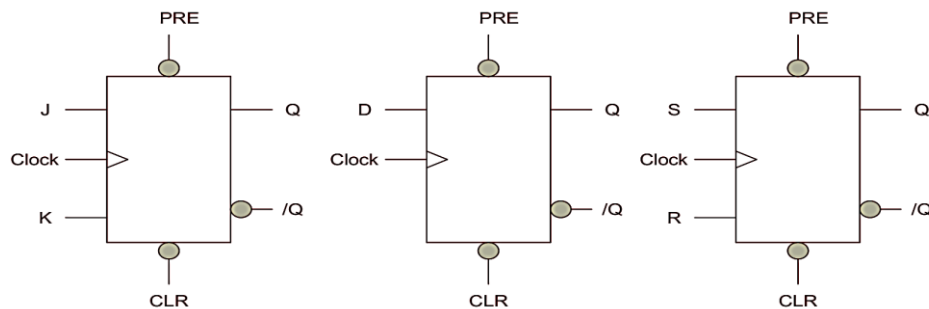


Figure 7.7: Asynchronous flip-flop's inputs.

When the preset input is activated, the flip-flop will be set ($Q = 1$, $/Q = 0$) regardless of the status of any of the synchronous inputs or the clock. When the clear input is activated, the flip-flop will be reset ($Q = 0$, $/Q = 1$) regardless of the status of any of the synchronous inputs or the clock.

If both preset and clear inputs are activated, we have an invalid state on the outputs where Q and $/Q$ go to the same state. Preset and clear inputs find their use in the designing of counters (asynchronous and synchronous).

Asynchronous inputs, just like synchronous inputs can be engineered to be active high or active low. If they are active low, there will be an inverting bubble at that input lead on the block symbol.



7.2.4 Monostable and astable multivibrator:

As we said above, a monostable multivibrator has only one stable state, the other state being momentary. An astable multivibrator has no stable state; it oscillates back and forth between two states. The integrated circuit NE555 is a multivibrator which can both function as monostable and as astable.

7.2.4.1 IC NE555:

The 555 integrated circuit is the most popular chip ever manufactured. Independently manufactured by more than 10 manufacturers, still in current

production, and almost 40 years old, this little circuit has withstood the test of time. It has been used in many things from toys to spacecraft. The IC 555 integrates a flip-flop circuit, and also operational amplifiers. The basic internal constitution of the IC 555 is given as follows.

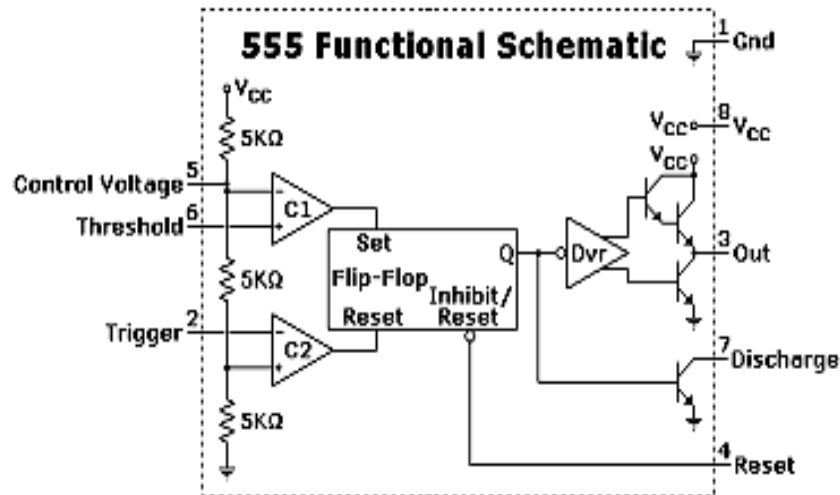


Figure 7.9: Internal diagram of the IC 555.

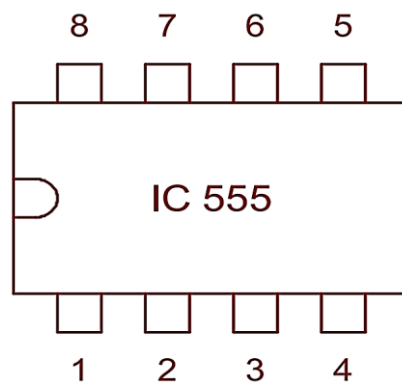


Figure 7.10: External appearance of the IC 555.

7.2.4.2 IC 555 as monostable:

A mechanical analogy of a monostable multivibrator would be a momentary contact push button switch which returns to its normal (stable) position when pressure is removed from its button actuator. In order to work as monostable multivibrator, the IC 555 should be connected as follows. The circuit is designed here using the electronic simulation software ISIS Professional edited by Labcenter. Values of component appearing on the diagram are just suggested.

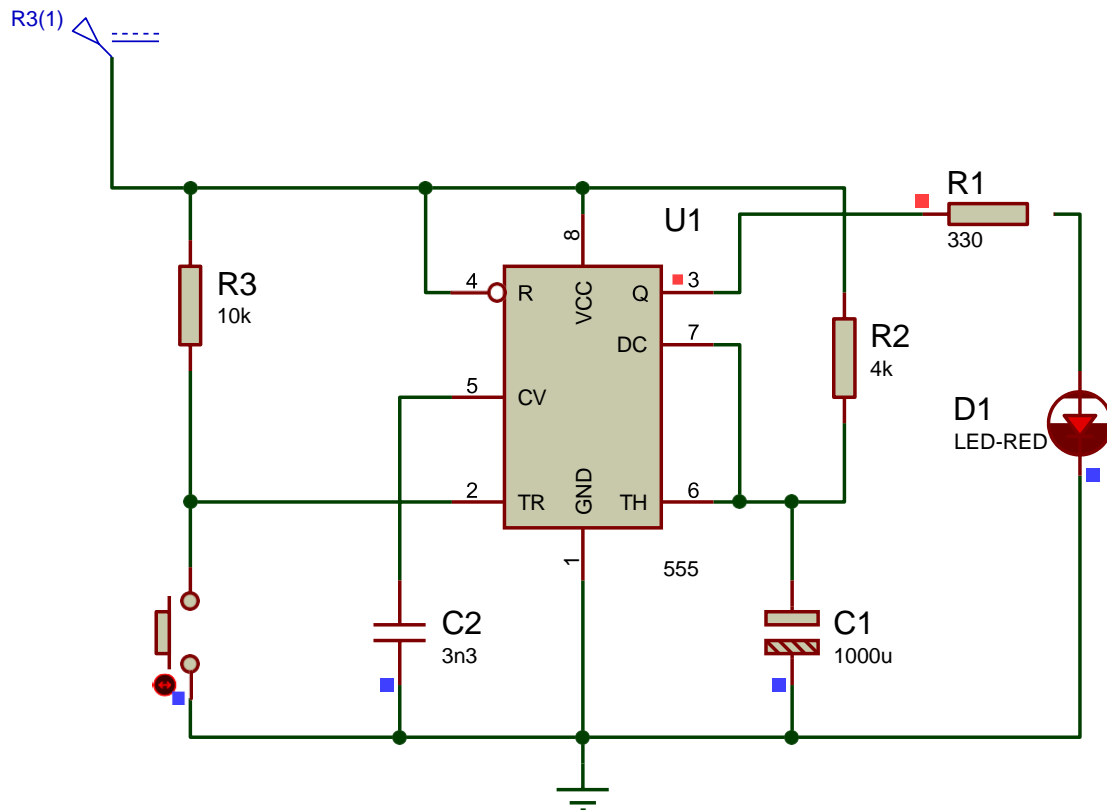
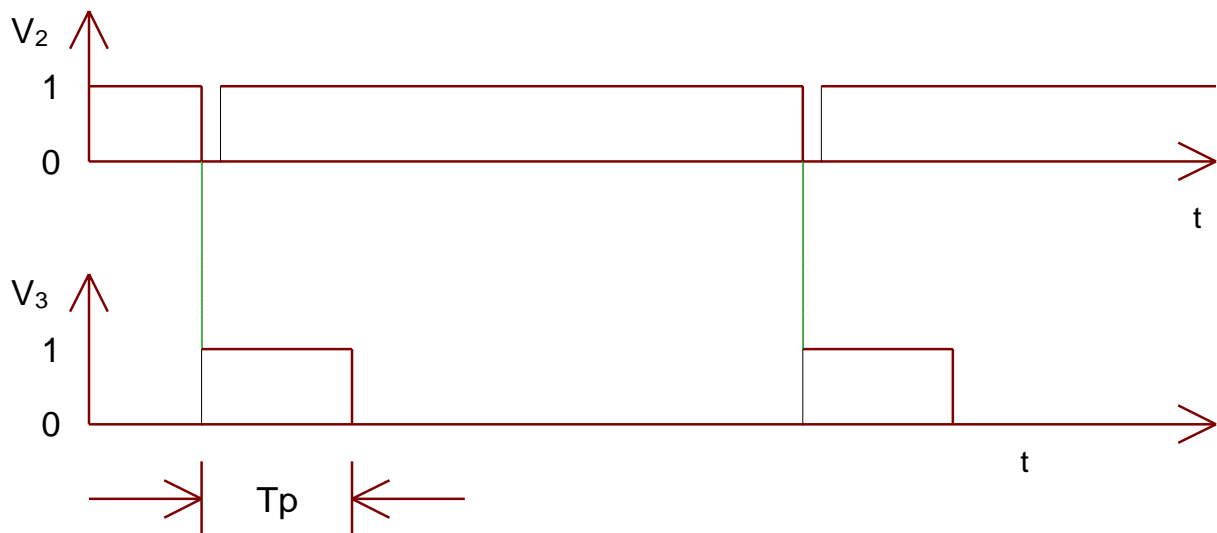


Figure 7.11: Simulation diagram for the IC 555 connected as monostable.

Probes 2 and 3 being respectively trigger and output, waveforms expected from them are as follows.



Anytime the circuit is triggered, that is by sending a brief low level logic signal at the lead number 2, the output 3 pass from its stable state which is low (0) to momentary high logic level that delays for a duration T_p . The duration T_p depends on the values of R_2 and C_1 and is given by the following formula.

$$T_p = R_2 C_1 \ln 3 = 1.1 R_2 C_1$$

For our example the duration of the temporisation T_p will be calculated as follows:

$$R_2 = 4k\Omega$$

$$C_1 = 1000\mu F$$

$$T_p = 4000 \times 1000 \times 10^{-6} \times 1.1 = 4.4$$

So, the duration of the temporisation is 4.4 seconds.

7.2.4.3 IC 555 as astable:

Astable multivibrator has no stable state and oscillates back and forth between an output of 0 and 1. In order to function as an astable, the IC 555 should be connected as follows:

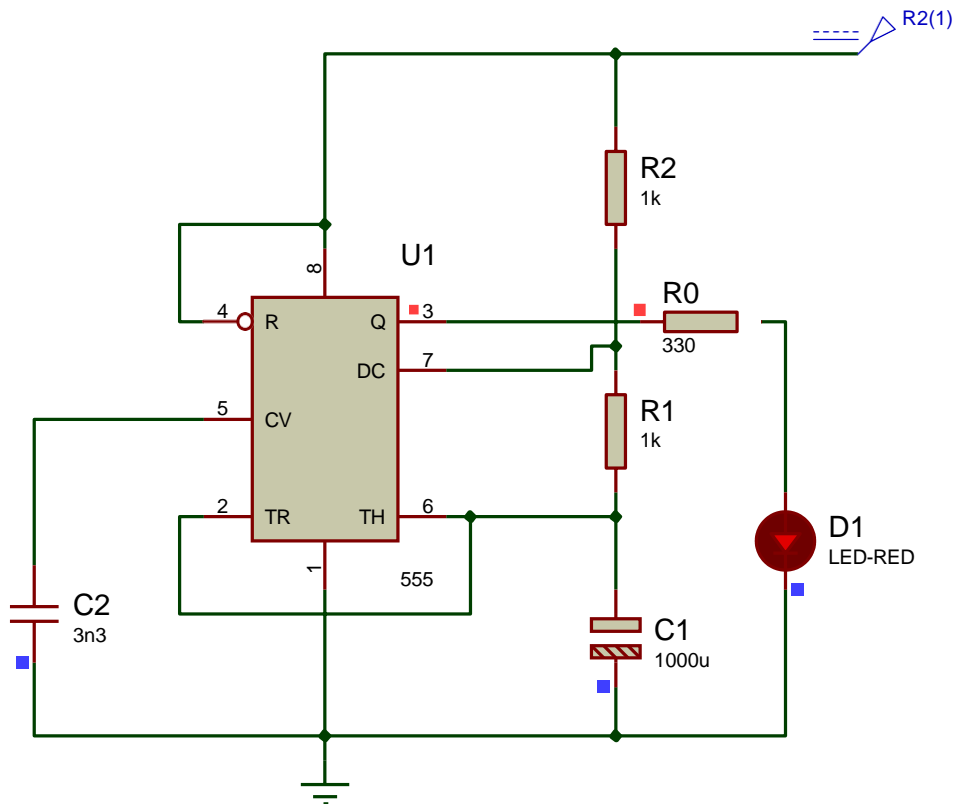
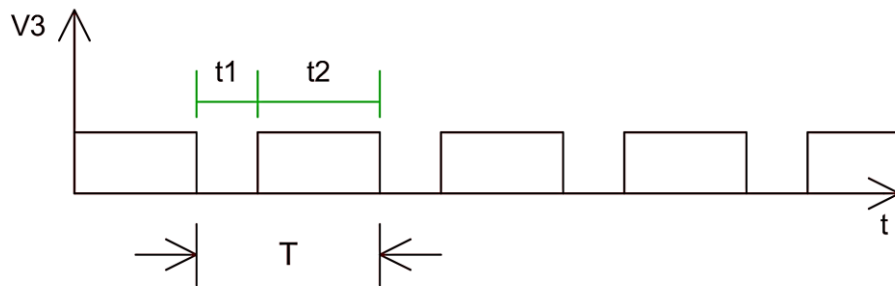


Figure 7.12: Simulation diagram for the IC 555 connected as an astable.

Once the circuit is supplied by a 5 V DC source, the output begins to oscillate between 0 and 1 logic levels. The led goes on and off alternatively. The waveform expected from the output is given as follows:



The period of the signal generated by the output is given as follows:

$$\begin{aligned}
 t_1 &= R_1 C_1 \ln 2 \\
 t_2 &= (R_1 + R_2) C_1 \ln 2 \\
 T &= t_1 + t_2 = (R_2 + 2R_1) C_1 \ln 2 \\
 T &= 0.693(R_2 + 2R_1) C_1
 \end{aligned}$$

For our example the duration of the period of the signal can therefore be calculated:

$$R_1 = R_2 = 1k\Omega$$

$$C_1 = 1000\mu F$$

$$T = 0.693 \times 3000 \times 1000 \times 10^{-6} = 2.079$$

So, the period of the signal generated by the output is 2.079 seconds.