Subtractors

Subtraction is the other basic function of arithmetic operations of information-processing tasks of digital computers. Similar to the addition function, subtraction of two binary digits consists of four possible elementary operations, which are 0–0 = 0, *0–1 = 1 with borrow of 1*, 1–0 = 1, and 1–1 = 0. The first, third, and fourth operations produce a subtraction of one digit, but the **second operation** produces a difference bit as well as a *borrow* bit. The borrow bit is used for subtraction of the next higher significant bit. A **combinational circuit** that performs the subtraction of ***two bits*** as described above is called a ***half-subtractor***. The digit from which another digit is subtracted is called the *minuend* and the digit which is to be subtracted is called the *subtrahend*.

When the minuend and subtrahend numbers contain more significant digits, the borrow obtained from the subtraction of two bits is subtracted from the next higher-order pair of significant bits. Here the **subtraction operation involves *three bits***—the minuend bit, subtrahend bit, and the borrow bit, and produces a different result as well as a borrow. The combinational circuit that performs this type of addition operation is called a ***full-subtractor***. Similar to an adder circuit, a full-subtractor combinational circuit can be developed by using two half-subtractors.

Design of Half-subtractors

A half-subtractor has two inputs and two outputs. Let the input variables minuend and subtrahend be designated as X and Y respectively, and output functions be designated as D for difference and B for borrow. The truth table of the functions is as follows.

Input variables		*Output variables*	
X	*Y*	*D*	*B*
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

By considering the minterms of the truth table, the Boolean expressions of the outputs D and B functions can be written as:

$D = X'Y + XY'$ and $B = X'Y$.

Figure 1 shows the logic diagram to realize the half-subtractor circuit.

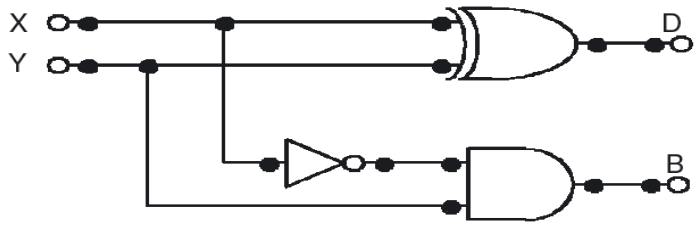

Figure (1)

Design of Full-subtractors

A combinational circuit of full-subtractor performs the operation of subtraction of **three bits**—the minuend, subtrahend, and borrow generated from the subtraction operation of previous significant digits and produces the outputs *difference* and *borrow*. Let us designate the input variables minuend as X, subtrahend as Y, and previous borrow as Z, and outputs difference as D and borrow as B. Eight different input combinations are possible for three input variables. The truth table is shown below according to its functions.

Input variables			*Outputs*	
X	*Y*	*Z*	*D*	*B*
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

	Y′Z′	Y′Z	YZ	YZ′
X′		1		1
X	1		1	

Figure 2(a) Map for function D.

	Y′Z′	Y′Z	YZ	YZ′
X′		1	1	1
X			1	

Figure 2(b) Map for function B.

Karnaugh maps are prepared to derive simplified Boolean expressions of D and B as in Figures 2(*a*) and 2(*b*), respectively.

The simplified Boolean expressions of the outputs are:

D = X′Y′Z + X′YZ′ + XY′Z′ + XYZ and

B = X′Z + X′Y + YZ.

The logic diagram for the above functions is shown in Figure 3.

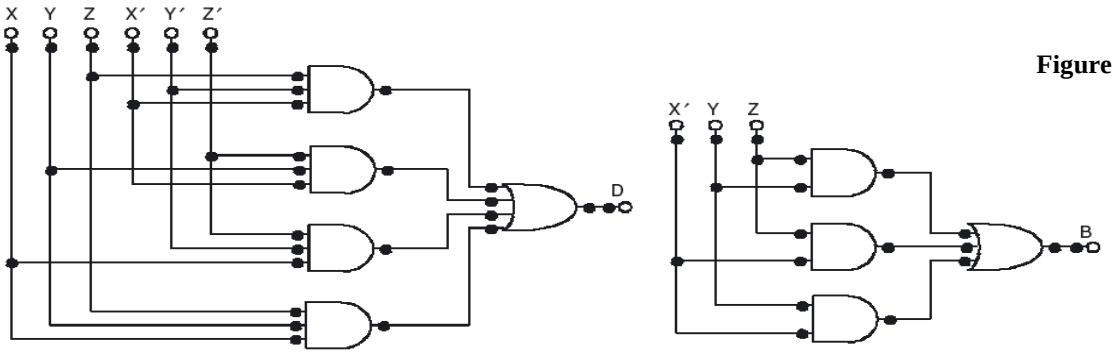

Figure 3

Similar to a full-adder circuit, it should be noticed that the configuration of the combinational circuit diagram for full-subtractor as shown in Figure 3 contains two-input and three-input AND gates, and three-input and four-input OR gates. Other configurations can also be developed where number and type of gates are reduced. For this, the Boolean expressions of D and B are modified as follows.

D = X′Y′Z + X′YZ′ + XY′Z′ + XYZ

= X′ (Y′Z + YZ′) + X (Y′Z′ + YZ)

= X′ (Y⊕Z) + X (Y⊕Z)′

= X⊕Y⊕Z

B = X′Z + X′Y +YZ = X′Y + Z (X′ + Y)

= X′Y + Z(X′Y + X′Y′ + XY + X′Y)

= X′Y + Z(X′Y + X′Y′ + XY)

= X′Y + X′YZ + Z(X′Y′ + XY)

= X′Y + Z(X⊕Y)′

Logic diagram according to the modified expression is shown in Figure 4.

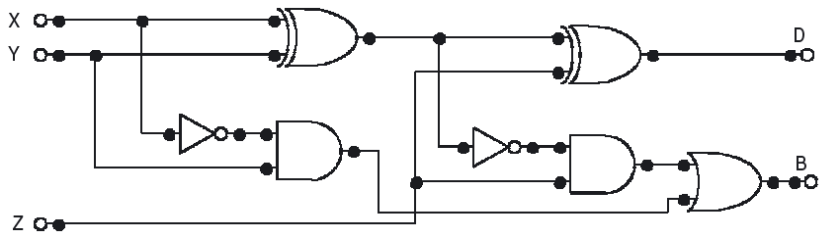

Figure 4

Note that the full-subtractor developed in Figure 4 consists of two 2-input AND gates, two 2-input XOR (Exclusive-OR) gates, two INVERTER gates, and one 2-input OR gate. This contains a reduced number of gates as well as type of gates as compared to Figure 3. Also, it may be observed, if compared with a half-subtractor circuit, the full-subtractor circuit can be developed with two half-subtractors and one OR gate.