Lecture 6: memory structure 8086

Outline:

1.introduction

2.memory reserve

3.bus operation

1.INRTODUCTION

The 8086 memory is a sequence of up to 1 million 8-bit bytes, a considerable increase over the 64K bytes in the 8080. Any two consecutive bytes may be paired together to form a 16-bit word. Such words may be located at odd or even byte addresses (16-bit references to odd locations require two hardware memory cycles, while those to even locations require just one). The most significant 8 bits of word are located in the byte with the higher memory address.

The 8086 memory may be conceived of as an arbitrary number of segments, each at most 64K bytes in size. Each segment begins at an address which is evenly divisible by 16 (i.e., the low-order 4 bits of a segment's address are zero). At any given moment the contents of four of these segments are immediately addressable. These four segments, called the current code segment, the current data segment, the current stack segment, and the current extra segment, need not be unique and may overlap. The high-order 16 bits of the address of each current segment are held in a dedicated 16-bit segment register and are called the segment address. In the degenerate case where all four segments start at the same address, namely address 0, we have an 8080 memory structure.

Bytes or words within a segment are addressed using 16-bit offset addresses within the 64K byte segment. A 20-bit physical address is constructed by adding the 16-bit offset address to the 16-bit segment address with 4 low-order zero bits appended. memory structure is shown in figure (1).

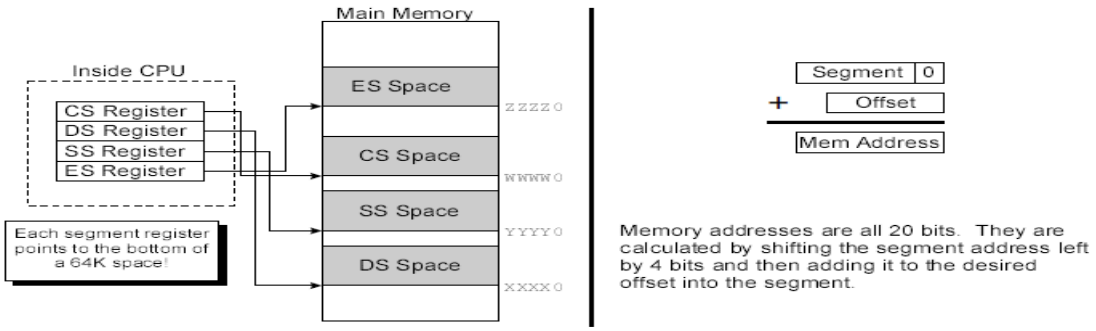


Figure 1: memory structure

For address and data operands (word 16 bit), the least significant byte of the word is stored in the lower valued address location and the most

significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte

boundary. Except for the performance penalty, this double access is transparent to the software. This performance penalty does not occur for instruction fetches, only word operands. Physically, the memory is organized as a high bank (D15-D8) and a low bank (D7-D0) of 512K 8-bit bytes addressed in parallel by the processor's address lines A19-A1. Byte data with even addresses is transferred on the (D7-D0) bus lines while odd addressed byte data (A0 HIGH) is transferred on the (D15-D8) bus lines. The processor provides two enable signals, BHE and A0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor to the byte level as necessary.

2.MMEMORY RESERVE

Certain locations in memory are reserved for specific CPU operations Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be.

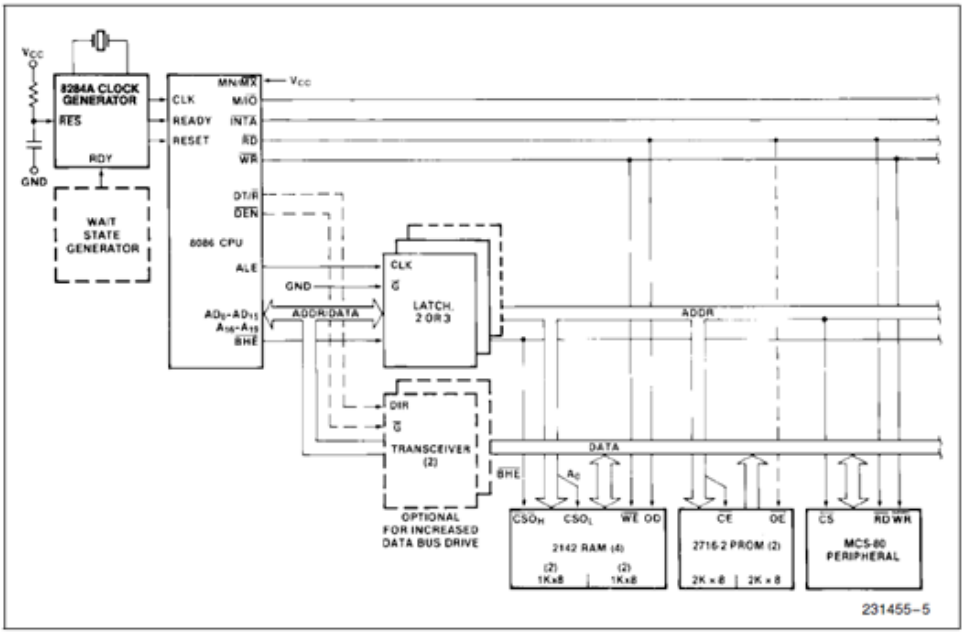
Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt types has its service routine pointed to by a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

2.1 Minimum and Maximum Modes

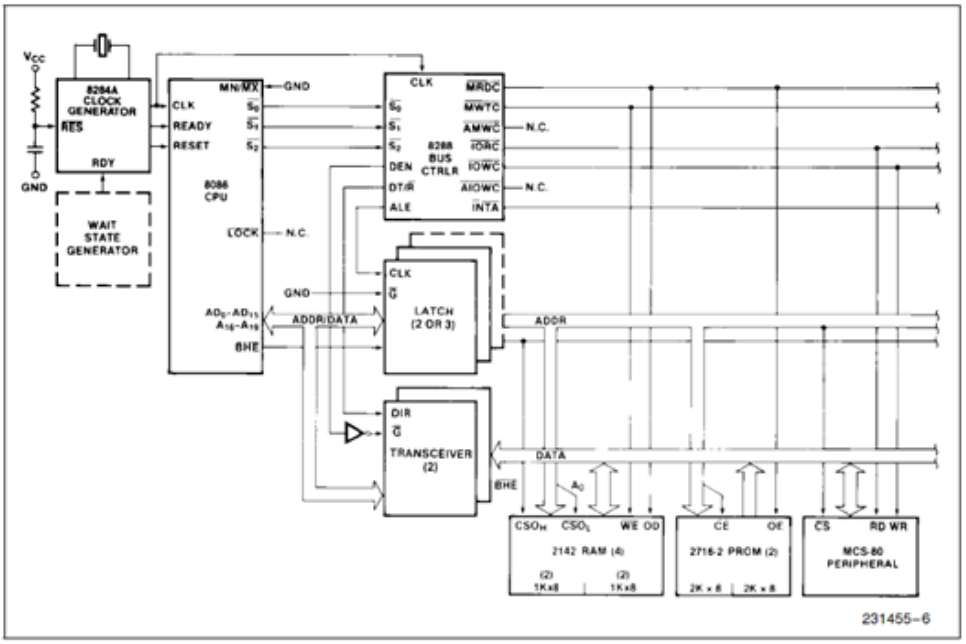
The requirements for supporting minimum and maximum 8086 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 8086 is equipped with a strap pin (MN/MX) which defines the system configuration.

The definition of a certain subset of the pins changes dependent on the condition of the strap pin. When MN/MX pin is strapped to GND, the

8086 treats pins 24 through 31 in maximum mode. An 8288 bus controller interprets status information coded into S0, S1, S2 to generate bus timing and control signals compatible with the MULTIBUS architecture. When the MN/MX pin is strapped to VCC, the 8086 generates bus control signals itself on pins 24 through 31. Examples of minimum mode and maximum mode systems are shown in Figure (2)



a. Minimum Mode 8086 Typical Configuration



b. Maximum Mode 8086 Typical Configuration

Figure 2:a-minimum mode , b-maximum mode

3.BUS OPERATION

The 8086 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This ``local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of address latches if a standard non-multiplexed bus is desired

for the system. Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4 which describe as follow :

- T1:The address is emitted from the processor.
- T2 is used primarily for changing the direction of the bus during read operations.
- T3 and T4: data transfer occurs on the bus during.
- Tw: Wait" states are inserted between T3 and T4. Each inserted ``Wait" state is of the same duration as a CLK cycle.

Periods can occur between 8086 bus cycles. These are referred to as ``Idle" states (Ti) or inactive CLK cycles. The processor uses these cycles for internal housekeeping. During T1 of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the 8288 bus controller, depending on the MN/MX strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched. Status bits S0, S1 , and S2 are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Characteristics
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S7 are multiplexed with high order address bits and the BHE signal, and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was used for this bus cycle in forming the address, according to the following table

S_4	S_3	Characteristics
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 is 0 and S7 is a spare status bit.