Lecture 4:8086 microprocessor

Outline:

1.introduction

2.8086 pins description

1.introduction

The 8086 was designed to provide an order-of magnitude increase in 8080. The processor was to be compatible with the 8080 at the assembly language level, so that existing 8080 software could be reassembled and correctly executed on the 8086.To allow for this, the 8080 register and instruction sets were to appear as logical subsets of the 8086 registers and instructions. By utilizing a general-register structure, Intel could capitalize on its experience with the 8080 to obtain a processor with a higher degree of sophistication.

The goals of the 8086 architecture were the symmetric extension of existing 8080 features and the addition of processing capabilities not found in the 8080. ***New features and capabilities included 16-bit arithmetic, signed 8- and 16-bit arithmetic (including multiply and divide), efficient interruptible byte-string operations, improved bit-manipulation facilities, and mechanisms to provide for re-entrant code, position-independent code, and dynamically relocatable programs. By now memory had become inexpensive and microprocessors were being used in applications requiring large amounts of code and data.*** Thus, another design goal was direct addressing of more than 64K bytes and support of multiprocessor configurations.

The 8086 processor architecture comprises *a memory structure, a register structure, an instruction set, and an external interface*. The 8086 can access up to one million bytes of memory and up to 64K input/output ports. The 8086 has three files of registers. ***One file contains general registers that hold intermediate results; the second contains pointer and index registers used to locate information within specified portions of memory; the third contains segment registers used to specify these portions of memory. The 8086 has nine flags that are used to record the state of the processor and to control its operations***. The 8086 instruction set and addressing modes are richer and more symmetric than the 8080. And the 8086 external interface, consisting of such things as interrupts, multiprocessor synchronization, and resource sharing, goes way beyond the facilities provided in the 8080.

The 8086 microprocessor features is shown in table (1), table (2) and table (3) compare to the 8008,8080 and 8085 microprocessors.

Table 1.
Feature comparison—Intel microprocessors, 1972-1978.

	8008	8080	8085	8086
INTRODUCTION DATE	1972	1974	1976	1978
NUMBER OF INSTRUCTIONS	66	111	113	133
NUMBER OF FLAGS	4	5	5	9
MAXIMUM MEMORY SIZE	16K BYTES	64K BYTES	64K BYTES	1M BYTES
I/O PORTS	8 INPUT 24 OUTPUT	256 INPUT 256 OUTPUT	256 INPUT 256 OUTPUT	64K INPUT 64K OUTPUT
NUMBER OF PINS	16	40	40	40
ADDRESS BUS WIDTH	8*	16	16	20*
DATA BUS WIDTH	8*	8	8	16*
DATA TYPES	8-BIT UNSIGNED	8-BIT UNSIGNED 16-BIT UNSIGNED (LIMITED) PACKED BCD (LIMITED)	8-BIT UNSIGNED 16-BIT UNSIGNED (LIMITED) PACKED BCD (LIMITED)	8-BIT UNSIGNED 8-BIT SIGNED 16-BIT UNSIGNED 16-BIT SIGNED PACKED BCD UNPACKED BCD
ADDRESSING MODES	REGISTER IMMEDIATE**	MEMORY DIRECT (LIMITED) MEMORY INDIRECT (LIMITED) REGISTER IMMEDIATE**	MEMORY DIRECT (LIMITED) MEMORY INDIRECT (LIMITED) REGISTER IMMEDIATE**	MEMORY DIRECT MEMORY INDIRECT REGISTER IMMEDIATE INDEXING

*ADDRESS AND DATA BUS MULTIPLEXED.
**MEMORY CAN BE ADDRESSED AS A SPECIAL CASE BY USING REGISTER M.

Table 2: performance evolution

	8008 (1972)	8080 (2 MHZ) (1974)	8086 (8 MHZ) (1978)
REGISTER-REGISTER TRANSFER	12.5	2	0.25
JUMP	25	5	0.875
REGISTER-IMMEDIATE OPERATION	20	3.5	0.5
SUBROUTINE CALL	28	9	2.5
INCREMENT (16-BIT)	50	2.5	0.25
ADDITION (16-BIT)	75	5	0.375
TRANSFERS (16-BIT)	25	2	0.25

ALL TIMES ARE IN MICROSECONDS.

Table 3: technology comparison

	8008 (1972)	8080 (1974)	8085 (1976)	8086 (1978)
SILICON GATE TECHNOLOGY	P-CHANNEL ENHANCEMENT LOAD DEVICE	N-CHANNEL ENHANCEMENT LOAD DEVICE	N-CHANNEL DEPLETION LOAD DEVICE	SCALED N-CHANNEL (HMOS) DEPLETION LOAD DEVICE
CLOCK RATE	0.5-0.8 MHz	2-3 MHz	3-5 MHz	5-8 MHz
MIN. GATE DELAY[1] FO = FI = 1	30 NS[2]	15 NS[2]	5 NS	3 NS
TYPICAL SPEED POWER PRODUCT	100 PJ	40 PJ	10 PJ	2 PJ
APPROXIMATE NUMBER OF TRANSISTORS[3]	2000	4500	6500	20,000[4]
AVERAGE TRANSISTOR DENSITY (MIL-SQRD PER TRANSISTOR)	8.4	7.5	5.7	2.5

NOTES:

1. FASTEST INVERTER FUNCTION AVAILABLE WITH WORST CASE PROCESSING.
2. LINEAR MODE ENHANCEMENT LOAD.
3. GATE EQUIVALENT CAN BE ESTIMATED BY DIVIDING BY THREE.
4. THIS IS 29,000 TRANSISTORS, IF ALL ROM AND PLA PLACEMENT SITES AVAILABLE ARE COUNTED.

2. 8086 pin description

8086 microprocessor shown in figure (1) and general mapping in figure(2). General 8086 microprocessor has 40 bins which is describes in table (4).

figure 1:8086 microprocessor imge

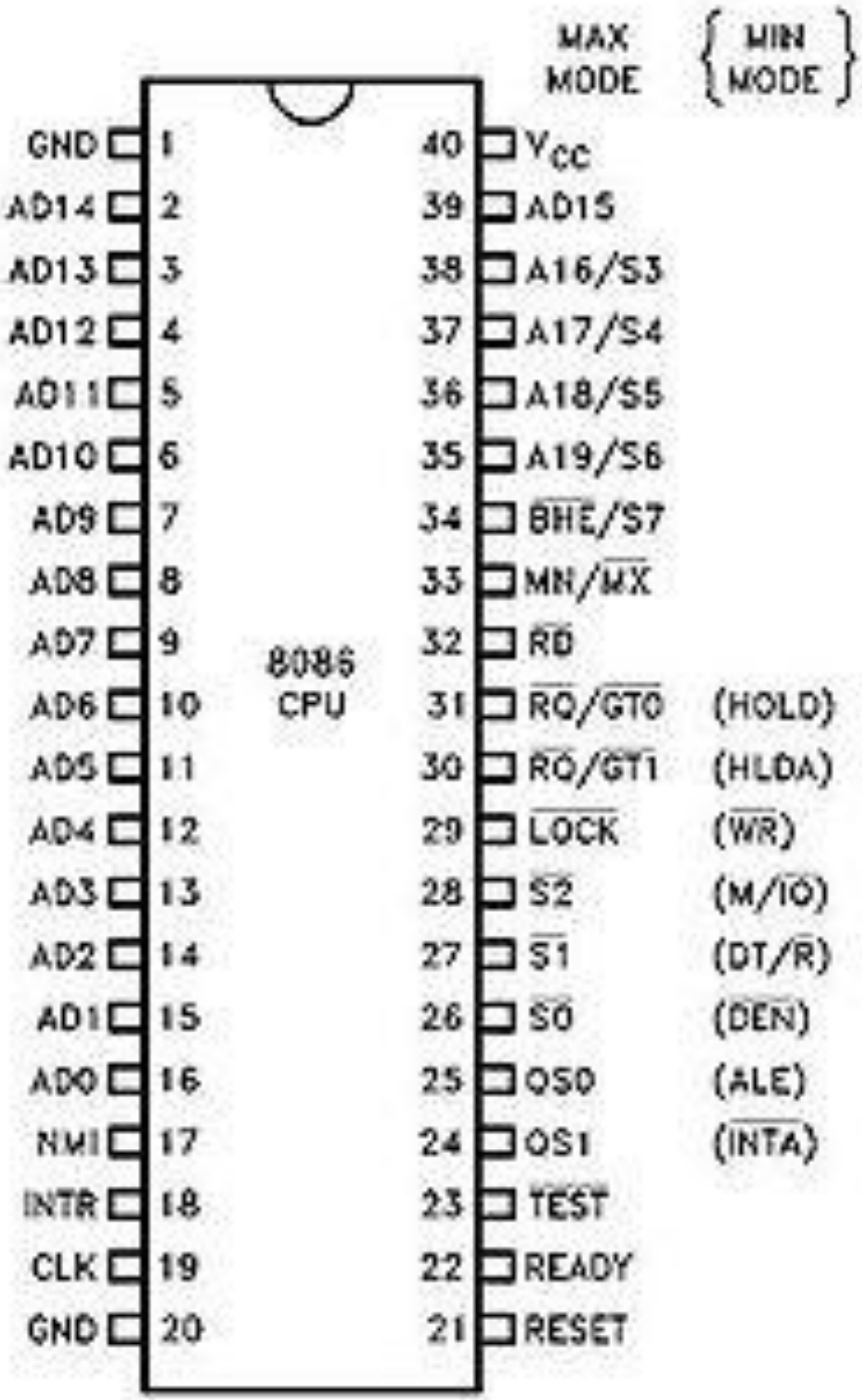
MAX MODE
MIN MODE
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
40 V_{CC}
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 $\overline{BHE}$/S7
33 MN/$\overline{MX}$
32 $\overline{RD}$
31 $\overline{RQ}$/$\overline{GT0}$ (HOLD)
30 $\overline{RQ}$/$\overline{GT1}$ (HLDA)
29 $\overline{LOCK}$ ($\overline{WR}$)
28 $\overline{S2}$ (M/$\overline{IO}$)
27 $\overline{S1}$ (DT/$\overline{R}$)
26 $\overline{S0}$ ($\overline{DEN}$)
25 QS0 (ALE)
24 QS1 ($\overline{INTA}$)
23 $\overline{TEST}$
22 READY
21 RESET
8086
CPU

Table 4.pin description

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$AD_{15}-AD_0$</td><td>2–16, 39</td><td>I/O</td><td>ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T_1), and data (T_2, T_3, T_W, T_4) bus. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7-D_0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions. (See $\overline{BHE}$.) These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus “hold acknowledge”.</td></tr>
<tr><td>A_{19}/S_6,
A_{18}/S_5,
A_{17}/S_4,
A_{16}/S_3</td><td>35–38</td><td>O</td><td>ADDRESS/STATUS: During T_1 these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W, T_4. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. A_{17}/S_4 and A_{16}/S_3 are encoded as shown.
This information indicates which relocation register is presently being used for data accessing.
These lines float to 3-state OFF during local bus “hold acknowledge.”
<table>
<tr><th>A_{17}/S_4</th><th>A_{16}/S_3</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>Alternate Data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>Code or None</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
<tr><td>S_6 is 0 (LOW)</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>$\overline{BHE}/S_7$</td><td>34</td><td>O</td><td>BUS HIGH ENABLE/STATUS: During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins $D_{15}-D_8$. Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S_7 status information is available during T_2, T_3, and T_4. The signal is active LOW, and floats to 3-state OFF in “hold”. It is LOW during T_1 for the first interrupt acknowledge cycle.
<table>
<tr><th>$\overline{BHE}$</th><th>A_0</th><th>Characteristics</th></tr>
<tr><td>0</td><td>0</td><td>Whole word</td></tr>
<tr><td>0</td><td>1</td><td>Upper byte from/to odd address</td></tr>
<tr><td>1</td><td>0</td><td>Lower byte from/to even address</td></tr>
<tr><td>1</td><td>1</td><td>None</td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$</td><td>32</td><td>O</td><td>READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the S_2 pin. This signal is used to read devices which reside on the 8086 local bus. $\overline{RD}$ is active LOW during T_2, T_3 and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the 8086 local bus has floated. This signal floats to 3-state OFF in “hold acknowledge”.</td></tr>
</table>

Symbol	Pin No.	Type	Name and Function
READY	22	I	**READY:** is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The READY signal from memory/ IO is synchronized by the 8284A Clock Generator to form READY. This signal is active HIGH. The 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
INTR	18	I	**INTERRUPT REQUEST:** is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{\text{TEST}}$	23	I	**$\overline{\text{TEST}}$:** input is examined by the "Wait" instruction. If the $\overline{\text{TEST}}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	**NON-MASKABLE INTERRUPT:** an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	**RESET:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	**CLOCK:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		**V_{CC}:** +5V power supply pin.
GND	1, 20		**GROUND**
MN/$\overline{\text{MX}}$	33	I	**MINIMUM/MAXIMUM:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the 8086/8288 system in maximum mode (i.e., MN/$\overline{MX}$ = V_{SS}). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

$\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$	26–28	O	**STATUS:** active during T_4, T_1, and T_2 and is returned to the passive state (1, 1, 1) during T_3 or during T_W when READY is HIGH. This status is used by the 8288 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$, or $\overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle.

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ (Continued)</td><td>26–28</td><td>O</td><td>These signals float to 3-state OFF in “hold acknowledge”. These status lines are encoded as shown.
<table>
<tr><th>$\overline{S_2}$</th><th>$\overline{S_1}$</th><th>$\overline{S_0}$</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
<tr><td>$\overline{RQ}/\overline{GT_0}$, $\overline{RQ}/\overline{GT_1}$</td><td>30, 31</td><td>I/O</td><td>REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor’s current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ pins have internal pull-up resistors and may be left unconnected. The request/grant sequence is as follows (see Page 2-24):
1. A pulse of 1 CLK wide from another local bus master indicates a local bus request (“hold”) to the 8086 (pulse 1).
2. During a T_4 or T_1 clock cycle, a pulse 1 CLK wide from the 8086 to the requesting master (pulse 2), indicates that the 8086 has allowed the local bus to float and that it will enter the “hold acknowledge” state at the next CLK. The CPU’s bus interface unit is disconnected logically from the local bus during “hold acknowledge”.
3. A pulse 1 CLK wide from the requesting master indicates to the 8086 (pulse 3) that the “hold” request is about to end and that the 8086 can reclaim the local bus at the next CLK.
Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.
If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:
1. Request occurs on or before T_2.
2. Current cycle is not the low byte of a word (on an odd address).
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.
If the local bus is idle when the request is made the two possible events will follow:
1. Local bus will be released during the next clock.
2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.</td></tr>
<tr><td>$\overline{LOCK}$</td><td>29</td><td>O</td><td>$\overline{LOCK}$: output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the “LOCK” prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in “hold acknowledge”.</td></tr>
</table>

Symbol	Pin No.	Type	Name and Function
QS_1, QS_0	24, 25	O	**QUEUE STATUS:** The queue status is valid during the CLK cycle after which the queue operation is performed. QS_1 and QS_0 provide status to allow external tracking of the internal 8086 instruction queue.

QS_1	QS_0	Characteristics
0 (LOW)	0	No Operation
0	1	First Byte of Op Code from Queue
1 (HIGH)	0	Empty the Queue
1	1	Subsequent Byte from Queue

The following pin function descriptions are for the 8086 in minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

M/$\overline{IO}$	28	O	**STATUS LINE:** logically equivalent to S_2 in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ floats to 3-state OFF in local bus "hold acknowledge".
$\overline{WR}$	29	O	**WRITE:** indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T_2, T_3 and T_W of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
$\overline{INTA}$	24	O	**$\overline{INTA}$:** is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3 and T_W of each interrupt acknowledge cycle.
ALE	25	O	**ADDRESS LATCH ENABLE:** provided by the processor to latch the address into the 8282/8283 address latch. It is a HIGH pulse active during T_1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	**DATA TRANSMIT/RECEIVE:** needed in minimum system that desires to use an 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{R}$ is equivalent to $\overline{S_1}$ in the maximum mode, and its timing is the same as for M/$\overline{IO}$. (T = HIGH, R = LOW.) This signal floats to 3-state OFF in local bus "hold acknowledge".
$\overline{DEN}$	26	O	**DATA ENABLE:** provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for INTA cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of T_2 until the middle of T_4, while for a write cycle it is active from the beginning of T_2 until the middle of T_4. $\overline{DEN}$ floats to 3-state OFF in local bus "hold acknowledge".
HOLD, HLDA	31, 30	I/O	**HOLD:** indicates that another master is requesting a local bus "hold." To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of a T_4 or T_i clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWer the HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold acknowledge (HLDA) and HOLD have internal pull-up resistors. The same rules as for $\overline{RQ}$/$\overline{GT}$ apply regarding when the local bus will be released. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.